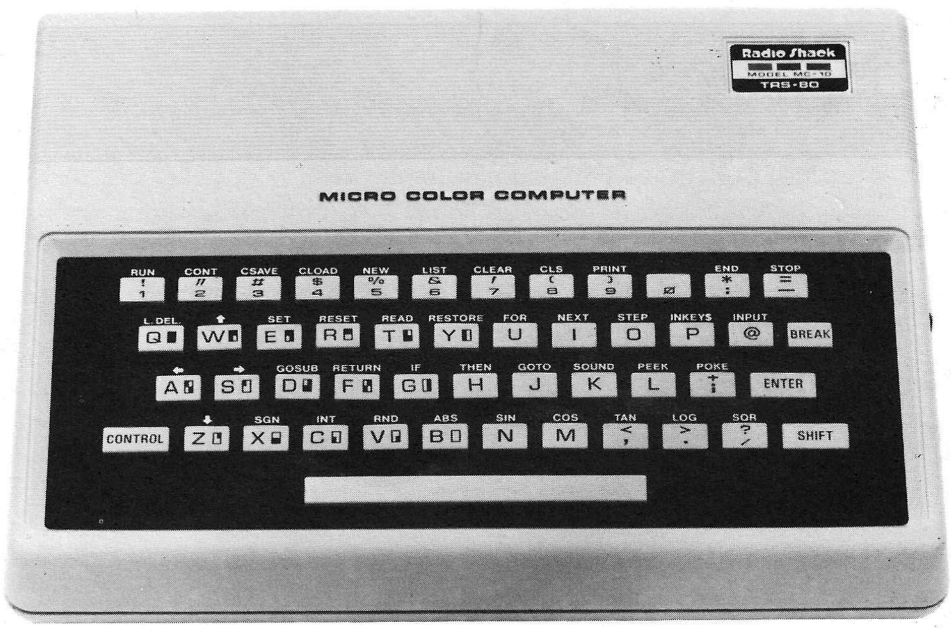
Radio Shack®

Service Manual

26-3011

TRS-80®
MICRO COLOR COMPUTER
PAL VERSION
MODEL MC-10
Catalog Number 26-3011



CUSTOM MANUFACTURED FOR TANDY CORPORATION

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SECTION I

SYSTEM DESCRIPTION

SYSTEM DESCRIPTION

The MC-10 Micro Color Computer is a fully expandable microprocessor system. It is composed of a 6803 central processing unit, 4K of static RAM, 8K of Basic ROM, and a 6847 video display generator. The microcomputer is also interfaced to a 48-key keyboard and provides the logic to execute a 1500 Baud cassette interface and a RS-232 serial interface. The system operates on a common color burst frequency of 3.579545 MHz. This main clock is divided by 4 in the CPU to yield an operating speed of 0.89 MHz.

In operation, the 4K of static RAM is shared between the CPU and the video display generator. This time multiplexing is based on the processor clock E. The CPU will be granted access to the RAM (upon request) only during the high state of E. This allows efficient usage of the RAM with no waiting by the CPU and no visible conflict on the display.

The 6847 VDG provides a display on a TV screen of 32 characters by 16 rows. It also allows a 64 x 32 semigraphics mode with eight colors. This display utilizes a minimum amount of system RAM (512 bytes).

The final elements of the microcomputer system are the I/O devices. The MC-10 is interfaced to a 48-key keyboard which generates the codes for upper and lower case characters, graphics symbols, and single stroke keyboard entry. The computer also provides a 1500 baud cassette interface for fast and reliable data and program storage and a limited signal RS-232C interface. The RS-232C interface allows either a printer or a modem to be used with the MC-10.

SYSTEM BLOCK DIAGRAM

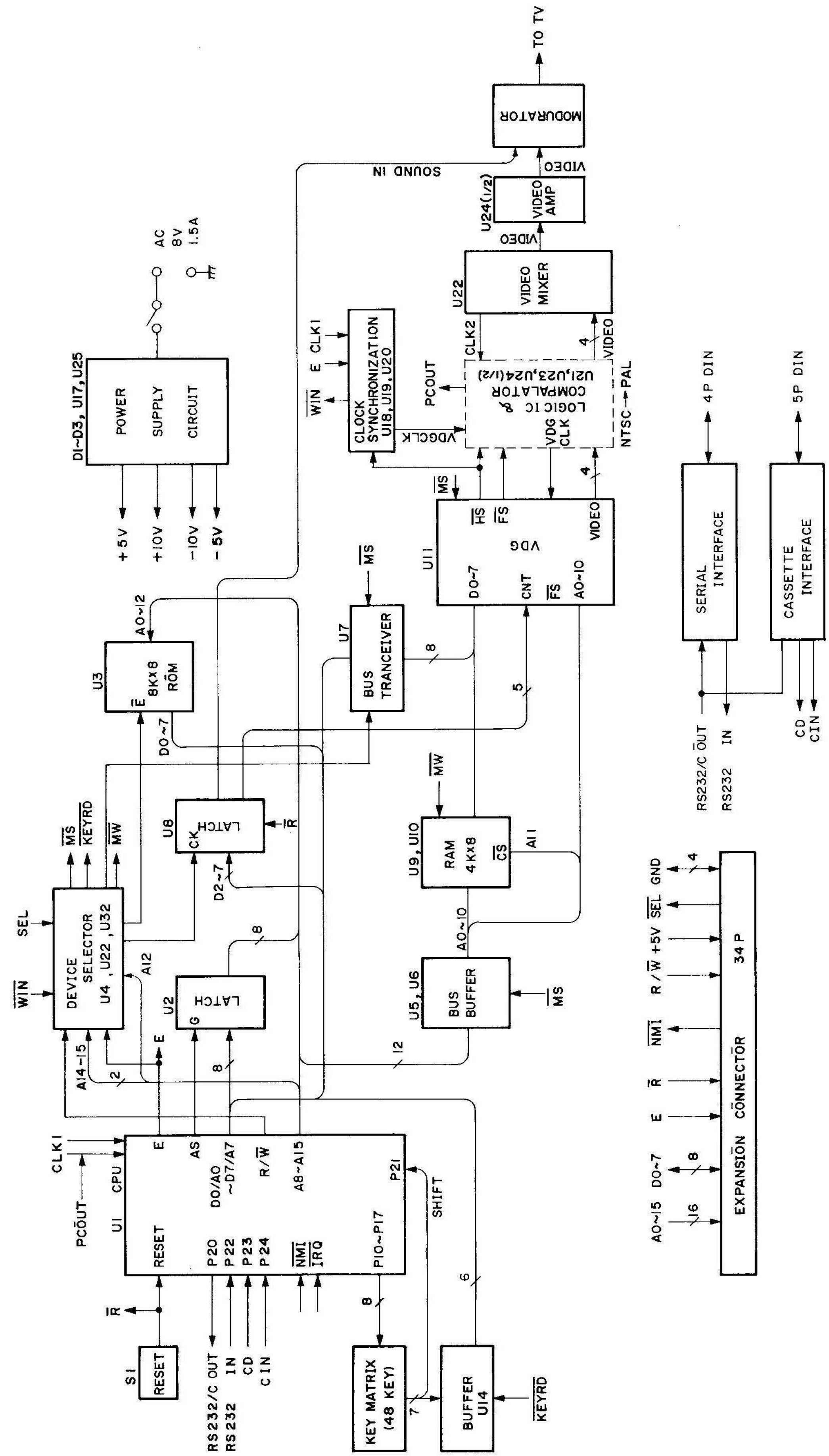


Figure 1

MEMORY MAP

Hex Address	
C000-FFFF	16K ROM (only 8K used)
9000-BFFF	16K I/O Slot (Keyboard and VDG control)
4000-8FFF	16K RAM (4K – 20K used)
0100-3FFF	Not Used
0080-00FF	RAM internal to the 6803
0015-007F	Not Used
0014	RAM Control Register
0013	Not Used
0012	Not Used
0011	Not Used
0010	Not Used
000F	Port 3 Control and Status Register
000E	Input Capture Register (low byte)
000D	Input Capture Register (high byte)
000C	Output Compare Register (low byte)
000B	Output Compare Register (high byte)
000A	Counter (low byte)
0009	Counter (high byte)
0008	Timer Control and Status Register
0007	Not Used
0006	Not Used
0005	Not Used
0004	Not Used
0003	Miscellaneous I/O Data Register
0002	Keyboard Output Lines
0001	Data Direction Register for miscellaneous I/O
0000	Data Direction Register for keyboard lines

SECTION II

SPECIFICATIONS

SPECIFICATIONS

Power Supply

AC/AC adaptor	Input	BG 220V/50Hz
		UKAU 240V/50Hz
	Output	8.0V/1.5A 22VA

RF Modulator		Ch.	FC (MHz)	Fsc (MHz)
BG	UHF	36	591.25 ±0.5	5.5 ±0.025
UK	UHF	36	591.25 ±0.5	6.0 ±0.025
Aust	VHF	1	57.25 ±0.3	5.5 ±0.025
		2	64.25 ±0.3	5.5 ±0.025

Output Impedance	75 ohm
RF Output Terminal	RCA jack

Central Processing Unit
- 6803 8-bit processor
- clock speed 0.89 MHz

Memory Size

ROM (for BASIC)	8K
RAM	4K (expandable up to 20K—external)

Video Display

Character display	512 (32 x 16) upper case characters
Semi-Graphic display	64 x 32 elements
Color	8 colors — Green, Yellow, Blue, Red, Buff, Cyan, Magenta, Orange

Interface

Printer	RS-232C, 4 pin DIN
Cassette	5-pin DIN 1500 baud
Bus line	34-pin Cartridge connector

Dimensions
- 8-1/2" x 1-7/8" x 7"

Weight
- 1.73 lbs (.7875 kilograms)

SECTION III

DISASSEMBLY/REASSEMBLY

DISASSEMBLY

1. Unplug the units from the AC wall outlet and disconnect all cables from the rear panel.
2. Turn the computer over and remove the four screws from the case bottom. One of the screws is located under the warranty seal in the upper right corner of the case bottom.
3. Turn the computer right side up. Disconnect the snap locks located on the right and left side of the case by placing a slotted screw driver in the groove between the top and bottom cases, approximately 2.7 inches from the rear of case. Push in and turn the screwdriver to pop the case apart.
4. Disconnect Keyboard cable from wire connector. NOTE: Pull flat wire upward.
5. Remove three screws that fasten the PC Board to the bottom of the case. Remove the PC Board.
6. Use tweezers to remove eleven clips that fasten the bottom shield to the P.C. Board.
7. Locate the eight positions where the top shield is soldered to the PC Board. Remove this solder with solder wick or a desoldering tool. Bend the protruding edge of the shield upward until it is parallel to the slot and remove top shield.

REASSEMBLY

1. Install the top PC Board shield. Solder the shield to the ground plane at eight points.
2. Install the bottom shield with metal side up. Secure to the PC Board with eleven clips.
3. Install PC Board in bottom of case. Secure with three screws.
4. Install the two keyboard cables in their respective connectors. This will be easier if both hands are used and you are facing rear of unit. Refasten cable restraints.
5. Join the top and bottom cases and push them together at the snap lock positions. This is a tight fit, therefore repositioning of the cases may be required.
6. Install four screws in bottom of case.

1. Removal of Top Cabinet

Remove 4 screws as shown in Figure A.

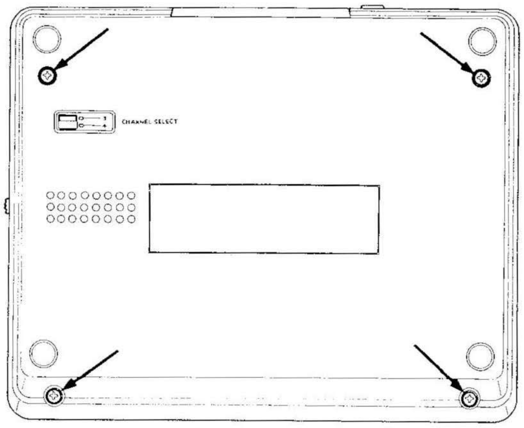


Figure A

2. Removal of P.C. Board

Remove flat wires of keyboard from connector.

Remove 3 screws as shown in Figure B.

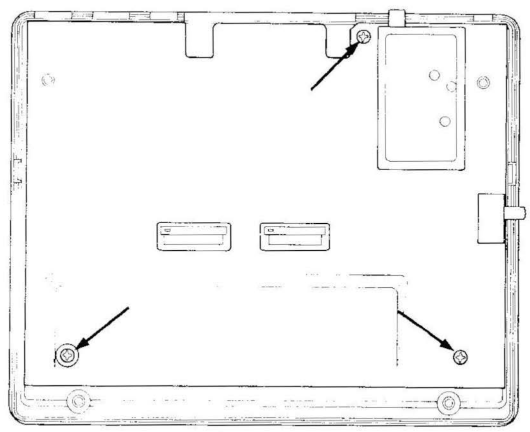


Figure B

3. Removal of Keyboard

Remove 4 screws as shown in Figure C.

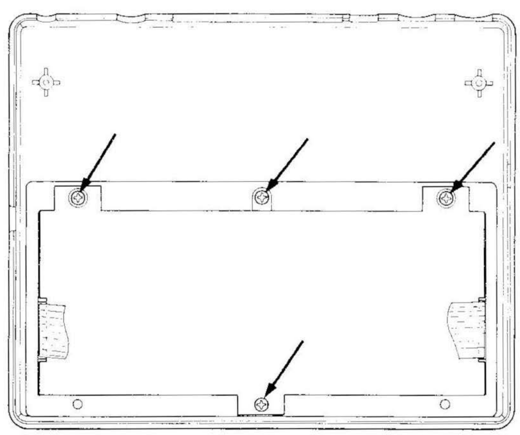


Figure C

SECTION IV

THEORY OF OPERATION

CPU-6803

The main component of this microcomputer system is the 6803 CPU. This is a 40-pin integrated circuit which provides the address, data, and miscellaneous control signals. The main clock frequency of 3.559383 MHz is produced by the oscillator circuit in the internal oscillator in the CPU, and X2, C39D12, divides this by 4 to produce an operating frequency of 0.89 MHz. This frequency is available as the processor clock E.

This processor chip is designed to be used in a minimum hardware configuration so I/O lines are provided directly from the CPU chip. In the MC-10 computer these I/O lines are used to address the keyboard and to support the cassette and RS232 interface.

The 6803 CPU is able to support several different modes of operation. For the MC-10 the CPU is operating in mode 2. The CPU mode is selected at power-up by the state of lines P20, P21, and P22. P20 and P22 are connected by a diode to Reset so that during power-up these lines are low. P21 is connected to a pull-up resistor so that during power-up it is high.

Mode 2 operates with 128 bytes of internal RAM, a full 16 line address bus and an 8 bit data bus which is multiplexed with the lower eight address lines. Due to the multiplexed address and data bus, two external devices are required. A 74LS373 is used to latch the address lines. This occurs during the low portion of the E clock when the CPU is not accessing external devices. The latch signal (AS) is provided by the CPU. The other external device is a 74LS245. This bi-directional buffer is required to isolate the RAM output lines, which are providing data to the video display generator during the low portion of the E clock, away from the CPU data bus. This buffer is controlled by the device selection logic.

RESET CIRCUIT

The reset circuit is composed of switch S1, diode D9, resistor R24, capacitor C8, and two gates of IC U12. R24 and C8 form a simple time constant so that during power up or whenever the reset switch is pressed, the reset line will stay low for a few milliseconds before returning to the high state. The reset input to the 6803 does not provide hysteresis so the reset signal must be buffered by U12 before being connected to the CPU. The final component of the circuit is diode D9 which is provided to allow for rapid cycling of the power switch.

ROM

The MC-10 uses a single 8K x 8 ROM to store the BASIC operating language. This is located in a 16K memory map segment between hex C000 – FFFF. This device is connected directly to the multiplexed address/data, however any possible contention is avoided by enabling the ROM only during the high cycle of the E clock.

CASSETTE INTERFACE

The cassette interface is composed of an output attenuator connected to a CPU output line and an input zero crossing detector. Most of the important cassette parameters are controlled by software. However, there is no cassette motor relay in the Micro Color Computer and cassette recorder operation must be manual.

The cassette format chosen uses a sinewave of 2400 or 1200 Hertz to yield a Baud rate of approximately 1500 Baud. In this format, a 0 (or logic low) is represented by one cycle of 1200 Hertz. A 1 (or logic high) is represented by one cycle of 2400 Hertz. A sample of data is shown in Figure 2. A typical program tape would consist of a leader of alternating 1's and 0's, followed by one or more blocks of data. A block of data is composed of 0 to 255 bytes of data with a checksum, sync byte, and the block length.

The output circuit utilizes a CPU output line to produce a sinewave of 1200 or 2400 Baud. This signal is then attenuated to approximately 1 volt and connected to the auxiliary input of the cassette recorder.

The input circuit is a zero crossing detector. R12 is a termination resistor for the cassette output. Resistors R16 and R17 are used to bias one input of the comparator at 1 volt. The other input is also biased at 1 volt by R15 and the series combination of R14 and R13. If the AC input from the recorder goes negative, diode D6 turns on and sets the input to the comparator equal to 1/2 volt. Since the other input is biased at 1 volt, the comparator output is switched to the high state. If the AC input from the recorder is positive, diode D6 is turned off and the input to the comparator will be at some point greater than 1 volt, in which case, the comparator output will be low.

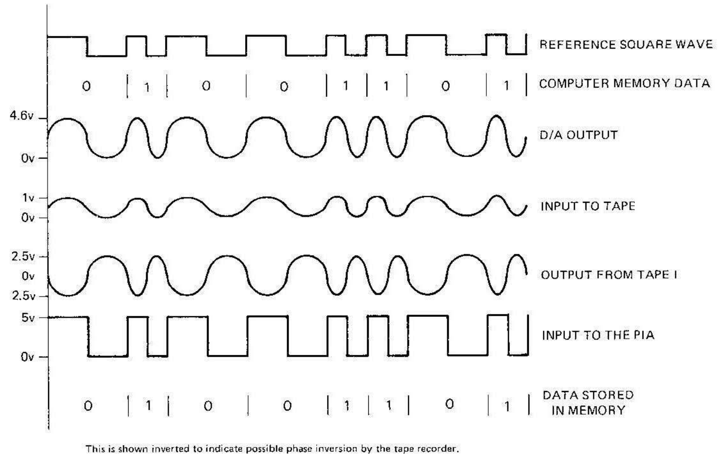


Figure 2. Sample Data of Cassette Format

The comparator output is open-collector so pull-up resistor R19 is provided to generate a TTL signal. R18 is used to prevent oscillation of the comparator. The final portion of the cassette circuit is capacitor C7 which is used to isolate RF noise from the cassette cable.

DETAILED TAPE FORMAT INFORMATION

The standard MC-10 tape is composed of the following items:

1. A leader consisting of 128 bytes of hex 55
2. A Namefile block
3. A blank section of tape approximately equal to 0.5 seconds in length; this allows BASIC time to evaluate the Namefile.
4. A second leader of 128 bytes of Hex 55
5. One or more Data blocks
6. An End of File block

The block format for Data blocks, Namefile blocks, or an End of File block is as follows:

1. One leader byte — 55H
2. One sync byte — 3CH
3. One block type byte — 01H = Data FFH = End of File 00H - Namefile
4. One block length byte — 00H to FFH
5. Data — 0 to 255 bytes
6. One checksum byte — the sum of all the data plus block type and block length
7. One leader byte — 55H

The End of File block is a standard block with a length of 0 and the block type equal to FFH.

The Namefile block is a standard block with a length of 15 bytes (OFH) and the block type equals 00H. The 15 bytes of data provide information to BASIC and are employed as described below:

1. Eight bytes for the program name
2. One file type byte — 00H = BASIC, 01H = Data, 02H = Machine Language
3. One ASCII flag byte — 00H = Binary, FFH = ASCII
4. One Gap flag byte — 01H = Continuous, FFH = Gaps
5. Two bytes for the start address of a machine language program
6. Two bytes for the load address of a machine language program

RS-232C INTERFACE

The RS-232C interface utilizes a 4-pin DIN connector (J2). This interface allows the computer to have serial communication with printers, modem, or other computers. The four signals used by the interface are:

1. CD — a status input line
2. RS232IN — serial data input
3. GROUND — zero voltage reference
4. RS232OUT — serial data out

The pin configuration for the DIN connector is shown in Figure 3.

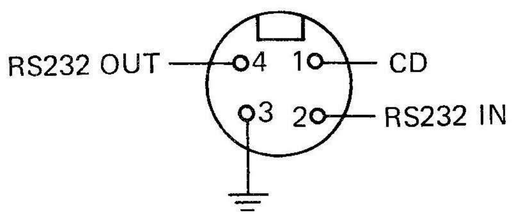


Figure 3. RS-232C Connector Pin-Out

In general, an RS-232C signal uses negative logic. Therefore, a voltage greater than +3 volts is defined as a SPACE, or logical 0. A voltage less than −3 volts is defined as a MARK, or logical 1. The range of −3 to +3 volts is undefined.

The RS-232C interface circuitry is shown on the upper right corner of the schematic. The output signal from the CPU output P20 is tied to a 741C op-amp (U16). This same output is also used for the cassette output, so care must be taken to ensure that a cassette output does not appear as an RS-232 output. The op-amp is referenced at 1.4 volts by resistors R2 and R3. This reference causes the op-amp to swing between the two power supply voltages (Vcc and Vee) as the TTL input switches states. A 100 ohm resistor (R1) is included to provide a current limit on the output. The two input signals (RS232IN and CD) utilize identical circuits and share a common bias resistor network. RS232IN (pin 4 of U15) is tied to CPU input P22 and CD (pin 6 of U15) is tied to CPU input P23. The inputs from the external device are connected to the positive side of a diode. This diode blocks the application of a negative voltage to the comparator (U15). When a positive voltage is applied, the diode conducts and the voltage is applied to the input. The comparators are referenced at two volts, by R5 and R6, thus if the input voltage is greater than 2.6 volts, the comparator is turned on. The comparator outputs are open-collector so pull-up resistors R8 and R9 are required.

I/O CONNECTOR

In addition to serial interfaces, the MC-10 also provides a full complement of CPU bus signals that are accessible at the 34-pin cartridge connector. This allows expansion of the MC-10 with external memory modules or ROM software modules. Table 1 provides a complete list of the signals and a brief description of each.

Table 1. I/O Connector Signals

Pin	Signal Name	Description
1	GND	Signal Ground
2	GND	Signal Ground
3	DO	CPU Data Bit 0
4	D1	CPU Data Bit 1
5	D2	CPU Data Bit 2
6	D3	CPU Data Bit 3
7	D4	CPU Data Bit 4
8	D5	CPU Data Bit 5
9	D6	CPU Data Bit 6
10	D7	CPU Data Bit 7
11	$R/\overline{W}$	CPU Read/Write Signal
12	A0	CPU Address Bit 0
13	A1	CPU Address Bit 1
14	A2	CPU Address Bit 2
15	A3	CPU Address Bit 3
16	A4	CPU Address Bit 4
17	A5	CPU Address Bit 5
18	A6	CPU Address Bit 6
19	A7	CPU Address Bit 7
20	A8	CPU Address Bit 8
21	A9	CPU Address Bit 9
22	A10	CPU Address Bit 10
23	A11	CPU Address Bit 11
24	A12	CPU Address Bit 12
25	A13	CPU Address Bit 13
26	A14	CPU Address Bit 14
27	A15	CPU Address Bit 15
28	E	Main CPU Clock (0.89 MHz)
29	SEL	Input to Disable Device Selection
30	RESET	Main Reset and Power-up Clear Signal to the System
31	$\overline{NMI}$	Non-Maskable Interrupt to the CPU
32	+5V	+5 volts (250 mA)
33	GND	Signal Ground
34	GND	Signal Ground

KEYBOARD INTERFACE

The Keyboard interface for the MC-10 utilizes the I/O lines of the 6803 CPU to reduce the logic required to a single six input CMOS buffer and seven pull-up resistors.

To read the keyboard, only one column is enabled by writing a zero to one of the eight CPU I/O lines that corresponds to that column, and by writing ones to all the other lines. If a key has been pressed in that column, one of the input lines will be a zero and the key location will correspond to the bit that is low. By scanning each column in the keyboard, all of the keys may be checked.

POWER SUPPLY

The MC-10 power supply utilizes an external power pack to supply 8 VAC at 1.5 amps. This input AC voltage is connected through the power switch to the bridge rectifier. The MC-10 operates primarily on +5 volts, so the negative output of the bridge is grounded to provide a larger current capability to the positive supply. The output from the bridge is filtered by C1 and C5 and is connected to the +5 volt regulator. The regulator provides +5 volts at a maximum of 1.5 amps to the digital circuitry.

A small amount of negative voltage is required to the RS-232 output op-amp. This current is supplied by the simple circuit composed of D2, D3, C3, C4, and C32. This circuit operates by using capacitor C3 for isolation from the primary bridge circuit. Then the negative voltage is rectified by D2 and D3. The negative supply voltage is then filtered by C4 and C32 before being connected to U16. This is an unregulated output. However, when coupled with the output from the main bridges, it provides a larger differential voltage (that is the source of the positive op-amp voltage) with no detrimental effects on the operation of the op-amp.

VDG

The video interface function in the MC-10 is performed by the MC6847. This is a flexible video display generator that will produce nine colors (eight colors and black), an alphanumeric display mode, and several high resolution graphics modes.

In the MC-10 the VDG is interfaced to 4K of static RAM and the mode control inputs are controlled by a 74LS174 register. However, the only modes of operation which are supported by the machine are the alphanumeric mode and the alpha semigraphic-4 mode. Table 4 lists all of the alphanumeric characters which may be displayed by the VDG along with the hex code which will produce the character. Table 2 lists the required control bit values to produce the MC-10 display modes.

In the MC-10 the 4K of RAM is shared between the CPU and video display generator. This is accomplished by providing buffers between the address lines (U5 and U6) the data line (U7), and synchronizing the operation of the VDG to the CPU.

Normally the three buffers are disabled so that the VDG address is being supplied to the RAM and the RAM data is supplied to the VDG. However, during a CPU access to the RAM, the three buffers are enabled and the MS* line is used to disable the address lines of the MC6847. This provides the CPU address to the RAM chips and allows a CPU read or write cycle to occur.

Table 2. VDG Control Register

Control Register Bits					DMA Bits		Mode Selected
D6 CSS	D5 A*/G	D4 GMD	D3 GM1	D2 GM2/ (INT*/EXT)	D6 INV	D7 A*/S	
0	0	X	X	0	0	0	Alphanumerical green
0	0	X	X	0	1	0	Alphanumerical inverted green
1	0	X	X	0	0	0	Alphanumerical orange
1	0	X	X	0	1	0	Alphanumerical inverted orange
X	0	X	X	0	X	1	Semigraphics Four

Table 3

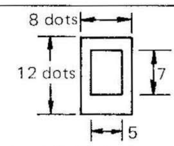
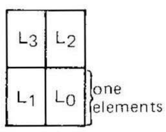
<table>
<tr><th colspan="2">VDG PINS</th><th colspan="3">COLOR</th><th colspan="2">TV SCREEN</th><th rowspan="2">VDG DATA BUS</th><th rowspan="2">COMMENTS</th></tr>
<tr><th>CSS</th><th>INV</th><th>Character Color</th><th>Background</th><th>Border</th><th>Display Mode</th><th>Detail</th></tr>
<tr><td rowspan="2">0</td><td>0</td><td>Green</td><td>Black</td><td rowspan="2">Black</td><td rowspan="2">32 Characters in columns</td><td rowspan="4"></td><td rowspan="4">| 0 | INV | | | | | | |
ASCII code</td><td rowspan="4">The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters @ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [/] ↑ ← SP ! " # $ % & ' + , - / 0 1 2 3 4 5 6 7 8 9 : 9 : ; - ?</td></tr>
<tr><td>1</td><td>Black</td><td>Green</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td>Orange</td><td>Black</td><td rowspan="2">Black</td><td rowspan="2">16 Characters in rows</td></tr>
<tr><td>1</td><td>Black</td><td>Orange</td></tr>
<tr><td>x</td><td>x</td><td>Lx C2 C1 C0
0 X X X
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0
1 1 0 1
1 1 1 0
1 1 1 1</td><td>Color
Black
Green
Yellow
Blue
Red
Buff
Cyan
Magenta
Orange</td><td>Black</td><td>64 Display elements in columns
32 Display elements in rows</td><td></td><td>| 1 | C2 | C1 | C0 | L3 | L2 | L1 | L0 |</td><td>The SEMIGRAPHICS FOUR mode uses an internal "coarse graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits. It requires 512 bytes of display memory.</td></tr>
</table>

Table 4. AVAILABLE CHARACTERS (00 – 7F)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	SPACE BAR	!	"	#	$	%	&	'	(	)	*	+	,	—	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	←
6	(@)	(A)	(B)	(C)	(D)	(E)	(F)	(G)	(H)	(I)	(J)	(K)	(L)	(M)	(N)	(O)
7	(P)	(Q)	(R)	(S)	(T)	(U)	(V)	(W)	(X)	(Y)	(Z)	([)	(\)	(])	(↑)	(←)

◯ = INVERTED CHARACTER
— = UNDEFINED

DEVICE SELECTION

A 74LS155 is used along with four OR gates and two inverters to provide device selection in the MC-10. The 74LS155 uses A15 and A14 to divide the memory map into four 16K segments. The bottom 16K segment is not used externally to the CPU. The next 16K segment is used for system RAM. The third 16K segment is used to read the keyboard and to write to the VDG control register. The final 16K is reserved for system ROM.

Both sections of the LS155 are used so that all of the device selects may be gated with E, while the CPU write signal for the RAMs is gated with window* (U18 pin 6). The disable inputs to the 74LS155 are tied through an inverter to the cartridge connector and to a pull-up resistor. This allows an external device to change the MC-10 memory map. Also, the disable signal for the memory write is ORed with A12 to prevent a complete overlap of the 4K of RAM into the 16K memory map segment.

From the output of the 74LS155 the IY1 output is used to switch the tri-state controls for the memory address and data buffers. The IY2 output is ORed with R/W and inverted R/W to provide a write pulse to the VDG control register (U8) and a read enable for the keyboard input buffer. The final output (IY3) is used to select the ROM chip.

SYSTEM TIMING

The main clock frequency of 3.559383 MHz is produced by the oscillator circuit in the CPU. This clock is buffered by one gate of U12 before being connected to the CPU and to the clock synchronization circuitry.

Internal to the CPU chip, the main clock frequency is divided by 4 to produce the processor clock E. This clock is used to synchronize all system operations to the CPU. Figure 5 shows the main clock and timing signals used in the MC-10.

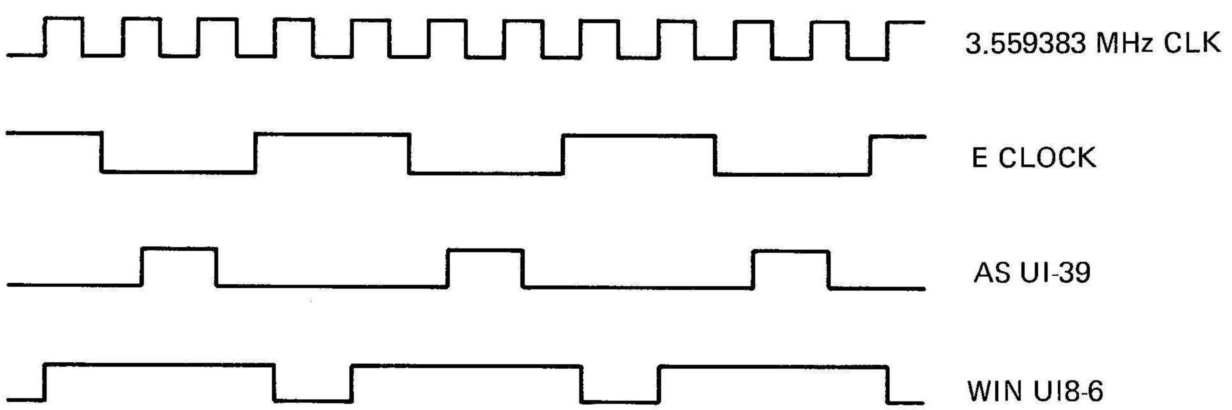


Figure 5

The MC6847 (VDG) has access to the RAM during the low portion of the E clock. Also during the low portion of E, the signal AS is used to latch the address lines in the latch (U2). During the high portion of E, all CPU address and data lines are valid and any accesses to the RAM or ROM occur during this time.

The signal window is used for two purposes. The first usage is to gate the write signal. The 2K x 8 static RAM requires setup and hold time on the address and data line, during a write cycle. The address and data lines are both valid for the high portion of the E clock. By gating the write pulse with window, a safety margin is created, so that the write pulse will never go low while the address or data is changing.

The second usage of the signal window is for synchronization of the VDG and the CPU. The two devices must be synchronized to allow both the CPU and the VDG to use the system RAM with no conflict. This has been accomplished in the MC-10 by forcing the VDG to latch data at the end of the low portion of the E clock. To do this, low transition of the signal HS* is only allowed to happen during the active portion of the signal window. If HS* occurs during the window, the latching of data will occur at the end of the low portion of the E clock.

RAM

The MC-10 uses two 2K x 8 static RAM chips for a total internal memory of 4K. The RAM chips receive their address lines from either the MC6847 (VDG) or the CPU. This switching is accomplished by tri-state buffers which are controlled by the MS* line. The individual RAM chip is selected by VA11 the 12th address line, and since the OE* input is grounded, one RAM is always enabled. The WE* line is generated by the CPU address decoding logic, and is high except when the CPU is writing to RAM.

PAL COLOR COMPUTER

The European and Australian version of the TRS-80 MC-10 is designed to produce a PAL system which modifies the NTSC signal to PAL signal.

The changes to the NTSC system may be divided into two categories.

1. Video changes — to produce a PAL compatible video signal.
2. Clock control circuitry — to synchronize the crystal oscillator circuits.

Use 3 ICs (U21 U23 U24) to modify the NTSC signal to PAL signal. The majority of the work is performed by U21, a gate array chip. Figure 7 shows a block diagram of this chip.

The basic differences between the PAL system and the NTSC system is that the PAL requires a 50 Hz line rate and a different color encoding scheme. The 50 Hz line rate is accomplished by stepping the clock to the MC6847 (U11). Normally the MC6847 generates 262 lines per field, but, due to the control function of U21, a total of 312 lines per field are generated in the PAL system. These added lines are partially visible as black stripes at the top and bottom of the video screen. The color encoding differences are handled by reconstructing the ØA signal.

The video circuitry of the PAL Color computer varies from the NTSC version only after the output of U11. The signals Y and ØB at the output of U11 are connected to a gate array chip. For Y (the composite video signal), the multiplexer gate is used to select a black-level, controlled by R31, 32, during the added 50 lines of video. For ØB (a color control signal), the multiplexer gate is used to add a color burst signal during the added 50 lines of video. The control signals are generated by logic inside the gate array chip, U21.

The other color control output from the MC6847 is ØA. For proper PAL color operation, this signal must be completely reconstructed by the gate array chip, U21. This is accomplished by translating the ØA signal from a three-level analog signal into digital inputs (+ØA and -ØA) for the gate array chip. This translation is accomplished by a high speed comparator, U23.

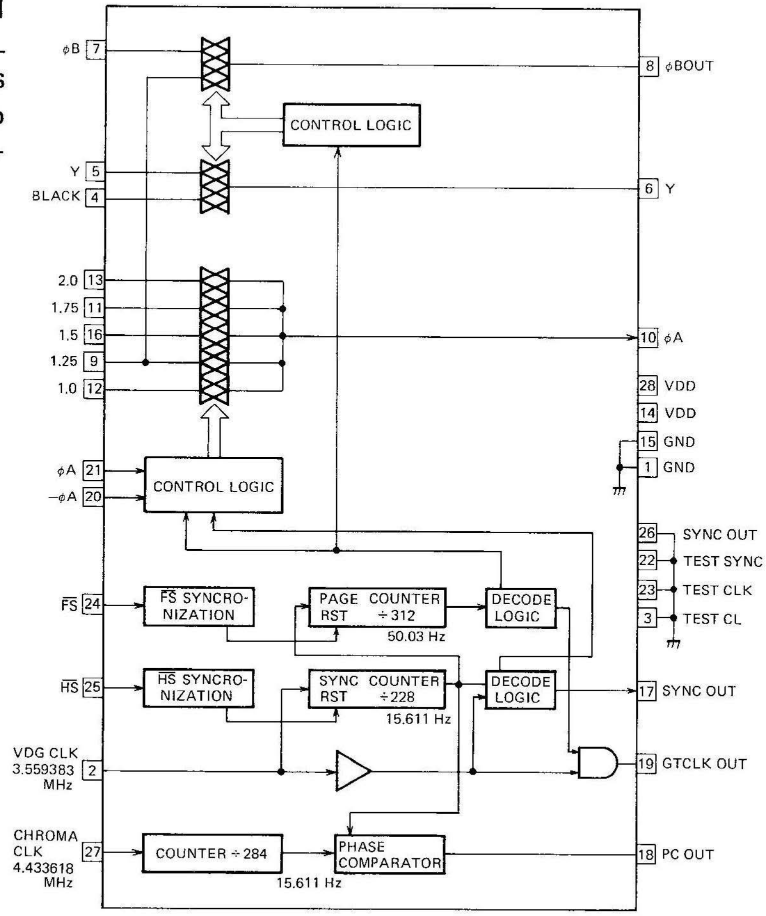


Figure 7. UA-2 8032000 BLOCK DIAGRAM

The signals +ØA and -ØA, once inside of U21, are combined with the color burst signal and the horizontal sync signal to produce the control signals for a four-input analog multiplexer, U22.

External to U21, a 4560 op-amp (U24) is used with a resistor network to produce the five DC reference voltages necessary for the reconstruction of ØA. These voltages are connected to the analog multiplexer gate inside of U21.

The remaining circuitry of U21 is used to produce the timing for the PAL translation process. This circuitry consists of two counters. The first counter is clocked by 3.55938 MHz from the CPU chip (U1) and divides this by 228 to count down to horizontal sync. The second counter is clocked by sync and divides this by 312 to count down to 50.03 Hz. Both counters are synchronized to the MC6847, U11 by sync pulses from that chip.

The final set of changes in the PAL Color computer is the addition of clock synchronization circuitry. In the PAL version, an extra crystal oscillator is needed for the PAL color burst frequency of 4.433618 MHz. For this purpose, the internal oscillator circuit of the MC1372, U22, is used. The addition of this crystal oscillator produces a color PAL video signal, but, due to the fact that the two oscillators are not synchronized, an apparent motion will exist whenever a color transition occurs.

This synchronization problem is solved by a slight shifting of the master oscillator frequency and the addition of a phase-locked-loop circuit. For the PAL version, the master crystal oscillator frequency is 3.55938 MHz. This allows the two oscillators to be divided down to the horizontal frequency of 15.611 Hz and phase-locked at this frequency.

The clock synchronization circuitry consists of IC U21. The PAL color burst frequency is 4.433618 MHz, which is divided by counter inside U21 by 284, to 15, 611 Hz. U21 also contains the phase comparator, and the sync signal generated from the master oscillator circuit (available at pin 17 of U21) is connected to the other phase comparator input. The phase comparator then generates a control voltage at the output, pin 18. This control voltage is passed through a simple R-C low pass filter and used to control a varactor diode D12. By varying the control voltage, the capacitance of the varactor may be changed to tune the master oscillator. This tuning allows the two oscillators to be synchronized at all times except during power-on.

ADJUSTMENTS

The PAL Color Computer has one adjustment to be made in the clock generation area. First adjust the frequency of the color burst (U22) oscillator by using a Frequency Counter at pin of U22 then adjusting C17 until the frequency is exactly 4.433618 MHz (±5 Hz).

At pin 28 of the VDG, the Y signal contains composite video and sync information. An example of this type of video signal is shown in Figure 8. This signal together with three color signals, CHB (pin 9), ØA (pin 11), and ØB (pin 10) is connected to the MC1372 color mixer chip U21 through PAL (Phase Alternating Line) system.

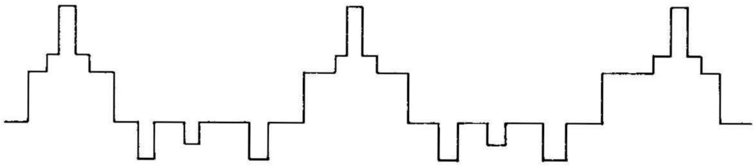


Figure 8. VDG VIDEO OUTPUT

The MC1372 is a complete color TV video modulator chip. However, for the MC-10 it is used as a color mixer chip. Figure 9 shows a block diagram of the MC1372 chip. Pins 1 and 2 of the MC1372 form an oscillator circuit. C17 is adjusted until the frequency of the color burst oscillator at pin 1 of U22 is exactly 4.433618 MHz.

The RF oscillator portion of the MC1372 is not required, so diode D10 and resistor R33 are used to kill the oscillation. Also the orientation of D10 controls the generation of normal of inverted video.

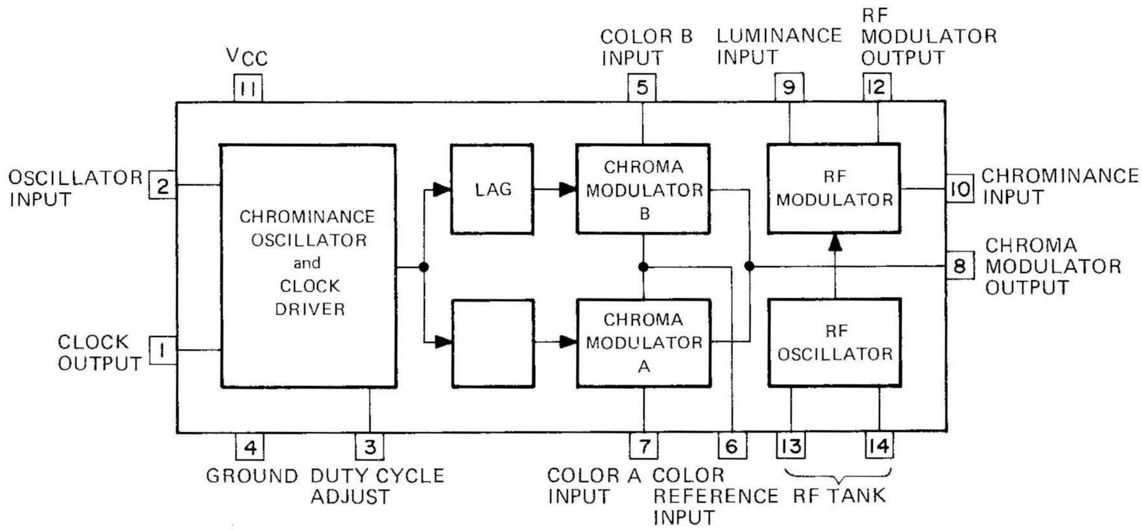


Figure 9. MC1372 BLOCK DIAGRAM

Using the color signals through PAL system from the VDG, U22 produces the chroma output at pin 8. This signal consists of the reference color burst and the video color information. The MC1372 requires this signal to be AC coupled to pin 10. This is accomplished by capacitor C38. Resistor R34 determines the Luminance to Chromance ratio.

The complete color video signal is available at pin 12 of the MC1372. However, at this point the signal has no drive capability and must be amplified before it can drive the modulator.

This amplification is accomplished by U24 and the associated circuitry.

The video amplifier is common collector amplifier designed to provide current gain. R37 and R38 form a voltage divider for the video input signal.

The video output from U24 is connected directly to video in of the modulator. The modulator also has sound capability which is used by the MC-10 is shown in Figure 10.

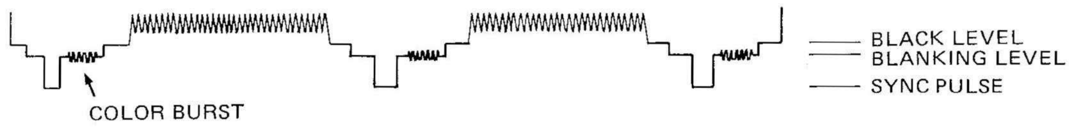


Figure 10. VIDEO INPUT TO THE MODULATOR

BG and UK models use UHF modulator. UHF modulator is single channel (36 CH). VHF modulator has channel select switch (S3). Channel 1 is selected by allowing the input to ground (57.25 MHz). Channel 2 is selected by +5V (64.25 MHz).

Internal to the modulator, the sound input signal is converted to a 5.5 MHz (for BG, Aust. models) and 6 MHz (for UK models) frequency modulated signal. This signal is then mixed with the video and used to modulate the RF signal for the selected channel. This final output is available at the phone jack connector of the modulator.
Table 5 shows the difference of all method.

Table 5

	DESTINATION	MODULATOR	CH	VIDEO CARRIER		SOUND CARRIER		
A	BG	UHF	36	591.25 MHz	±5	5.5	±0.025	
	UK	UHF	36	591.25 MHz	±5	6.0	±0.025	
B	Aust.	VHF	1	57.25 MHz	±0.3	5.5	±0.025	SW3
			2	64.25 MHz	±0.3	5.5	±0.025	

NOTE:
If the video display assembly is found to be faulty, replace it. Do not attempt to repair it.

SECTION V

TROUBLESHOOTING

TROUBLESHOOTING

Problems with the MC-10 may be separated into two major areas — I/O problems and dead computer problems. If the computer will display the sign-on message, then a fairly simple set of testing procedures may be used to isolate the problem. If, however, the computer displays random characters on the screen or has no display, then a major failure has occurred.

In the case of a major failure, the first thing to check is the +5-volt power supply. If the voltage level is off by more than 10%, then the power supply is the problem. Refer to the Power Supply section for hints on how to isolate the problem.

If the power supply has a proper +5 volts output, then check the clock output from the modulator at U12 pin 13. If the clock is oscillating at the proper frequency, and you have no display, the problem is in the video area. Refer to the section on the video interface for hints on fixing this problem.

If the MC-10 displays garbage on the screen, then some problem is causing a failure of the CPU. At this point you will have to remove the top and bottom shield. After you have removed the two shields, test the operation of the MC-10 to be sure that the problem was not a short to the shield.

With both of the shields removed, check the address and data lines of the 6803. After the reset switch has been pressed, check for indications that the CPU is operating. If the CPU shows no signs of activity, then one of the input signals is preventing the CPU from operating or the CPU is bad.

If the CPU is operating, then the most likely problems are a memory or buffer chip failure or a short on the address or data bus. In this case you will have to methodically check the address and data lines, while looking for a line that shows a problem.

In the case of a simple I/O problem, please refer to the appropriate interface section discussion.

VIDEO INTERFACE

Almost all of the work for the video interface is performed by the VDG (U11 — MC6847). Therefore, this chip is the most likely source of a video problem. However, it is always a good idea to isolate the source of a problem before trying to desolder chips.

If the problem is no picture or a distorted picture, then a new switch box and cable should be tried. If you still do not have a picture, then use an oscilloscope to look at U11 pin 28. You should have a video signal at this point. If you do not have a video signal, check +5 volts (pin 17) and the 3.559 MHz clock (pin 33), if you have both of these inputs and no video out, then U11 is bad.

If you have a video signal at pin 28, but no picture on your TV, then there could be a problem with the modulator. Check the +5-volt input before replacing the modulator.

The only other type of video failure which can occur in the MC-10 is the loss of synchronization with the CPU which will cause excess glitches on the screen. If this occurs, then the circuitry composed of U18 and U19 is failing.

KEYBOARD INTERFACE

The keyboard interface is composed of one resistor pack and one IC (U14). A keyboard failure will usually be caused by a mechanical failure of the keyboard, or a short or open in the cable. Mechanical failures will usually be only one or two isolated keys failing. Cable failures will cause an entire keyboard row or column to fail.

RS-232 INTERFACE

The RS-232 interface uses three simple level converter circuits. Isolating the problem will be an easy job of comparing the input to the output.

Connect a DIN-type plug to the serial I/O jack to short together pins 1, 2, and 4. Now, type in the following test program:

```
 5  POKE 3, 1
10  FOR X=0 TO 10: NEXT X
15  POKE 3, 0
20  FOR X=0 TO 10: NEXT X
25  GOTO 5
```

Run the program and check pin 2 of U16; a switching TTL waveform should be present. Pin 6 of U16 should have the same waveform except that it will be switching from +Vcc to -Vcc (the supply voltages of pins 4 and 7 of U16). Also check pins 4 and 6 of U15. These pins have the same waveform switching from 0 to +Vcc. The outputs of U15, pins 1 and 2 should show the original TTL signal.

CASSETTE INTERFACE

If you are having problems with the cassette circuit, short together pins 4 and 5 of the cassette DIN plug. Next run the program listed for the RS-232 interface test. The output pin is shared between RS-232 and cassette, so this test program will produce a switching TTL waveform on the output.

The output circuit is a simple attenuator, so the likely failure here should be a short to ground. The output on pin 5 of the DIN connector should be switching for 0 to +1 volt.

The input circuit is a zero crossing detector. It should convert the cassette signal back to the original TTL waveform at pin 13 of U15.

POWER SUPPLY

The power supply circuit in the MC-10 has a minimum component count so that a failure should be readily identifiable.

The first place to check if the computer has no +5-volt supply voltage is the output of the regulator. With the power pack unplugged, measure the resistance between the +5 output and ground. If this shows zero resistance, the problem is a short to ground.

If the +5 output is not shorted, check the voltage with the power pack plugged in. You should have 8 VAC at the power ON-OFF switch. If this looks good, check the input to the regulator. Here you should see a full wave rectified voltage of 10 volts DC. If you do not, one of the following components could be bad: D1; CI or C5; U15, U16, or U17.

The only major remaining component is the +5-volt regulator. If the regulator is receiving the proper input voltage, and there is no +5 volts, the regulator chip is bad.

Also, there is a simple circuit to supply an unregulated negative voltage to the RS-232 interface. If you are missing the negative voltage but the +5 volts is OK, then one of the diodes or the capacitors has failed.

SECTION VI

PARTS LIST

ELECTRICAL PARTS LIST

CAPACITORS

Ref. No.	Material	Value (μF)	Voltage (V)	Tolerance (%)	Mfr's Part No.
C1	Electrolytic	6800	16	±20	
C2	Electrolytic	10	25	±20	
C3/4	Electrolytic	470	16	±20	
C5	M-Plastic Capacitor	0.1	50	±5	
C6	Ceramic	0.0022	50	+80/–20	
C7	Ceramic	0.022	50	+80/–20	
C8	Electrolytic	4.7	50	±20	
C9–12	Ceramic	0.022	50	+80/–20	
C13	M-Plastic Capacitor	0.1	50	±5	
C14	Ceramic	0.022	16	±30	
C15/16	M-Plastic Capacitor	0.1	50	±5	154010240A
C17	Trimmer	50p	50	+100/–0	
C18	M-Plastic Capacitor	0.1	50	±5	
C19	Ceramic	0.022	16	±30	
C20–23	M-Plastic Capacitor	0.1	50	±5	
C24/25	Ceramic	0.022	16	±30	
C26–31	M-Plastic Capacitor	0.1	50	±5	
C32	Ceramic	0.022	16	±30	
C33	Electrolytic	1	50	±20	
C34	M-Plastic Capacitor	0.1	50	±50	
C35	Ceramic	0.022	16	±30	
C36	M-Plastic Capacitor	0.1	50	±5	
C37	Ceramic	39p	50	±5	
C38	M-Plastic Capacitor	0.1	50	±5	
C39	Ceramic	36p	50	±5	
C40	Not Used				
C41	Ceramic	0.001	50	+80/–20	
C42	Mylar	0.001	50	±5	
C43	Tantalum	0.47	25	±20	
C44	Ceramic	12p	50	±5	
C45	M-Plastic Capacitor	0.1	50	±5	
C46	Ceramic	0.022	16	±30	
C47	Not Used				
C48	Electrolytic	10	16	±20	
C49	Ceramic	0.022	16	±30	
C50	Electrolytic	10	25	±20	

DIODES

Ref. No.	Description		R/S Part No.	Manufacturer
D1	ID4B42 or	RECTIFIER		TORSHIBA
D1	DBB10B	RECTIFIER		SANYO
D2/3	10E1 or	SI DIODE		NIHONINTER
	SR1K-2	SI DIODE		UNIZON
D4–11	1N4148	SI DIODE		HITACHI
D12	ITT-310S	VARICAP		ITT

CORE

Ref. No.	Description	R/S Part No.	Mfr's Part No.
FB1–5	CORE ϕ3.5x1.3x5 or BL01RN1-A61		588010050A 588010060A

CONNECTORS

Ref. No.	Description	R/S Part No.	Mfr's Part No.
J1	5P TCS4450-01-1011		193410030A
J2	4P TCS4440-01-1011		193410020A
J3	POWER JACK		196610020A
J4/5	WIRE CONNECTOR		193904400A

INDUCTOR

Ref. No.	Description	R/S Part No.	Mfr's Part No.
L1	Inductor		142011510A

RESISTORS

Ref. No.	Material	Value (ohm)	Wattage (W)	Tolerance (%)	Mfr's Part No.
R1	Carbon	100	½	±5	
R2	Carbon	3.9K	¼	±5	
R3	Carbon	1.5K	¼	±5	
R4	Carbon	10K	¼	±5	
R5	Carbon	15K	¼	±5	
R6/7	Carbon	10K	¼	±5	
R8/9	Carbon	4.7K	¼	±5	
R10	Carbon	75K	¼	±5	
R11	Carbon	24K	¼	±5	
R12	Carbon	220	¼	±5	
R13	Carbon	8.2K	¼	±5	
R14	Carbon	6.8K	¼	±5	
R15/16	Carbon	56K	¼	±5	
R17	Carbon	15K	¼	±5	
R18	Carbon	1.5M	¼	±5	
R19	Carbon	4.7K	¼	±5	
R20	R-BLOCK	10K	½	±5	522110130A
R21–23	Carbon	4.7K	¼	±5	
R24	Carbon	100K	¼	±5	
R25	Carbon	4.7K	¼	±5	
R26–29	Carbon	30	¼	±5	
R30	Carbon	120	¼	±5	
R31	Carbon	4.7K	¼	±5	
R32	Carbon	5.1K	¼	±5	

Ref. No.	Material	Value (μF)	Voltage (V)	Tolerance (%)	Mfr's Part No.
R33	Carbon	750	¼	±5	
R34	Carbon	1K	¼	±5	
R35	Carbon	1.2K (1.1K-1.3K)	¼	±5	
R36	Carbon	5.6K	¼	±5	
R37	Carbon	470K	¼	±5	
R38	Carbon	270K	¼	±5	
R39/40	Carbon	10K	¼	±5	
R41	Carbon	100	¼	±5	
R42	Carbon	1K	¼	±5	
R43	Carbon	33K	¼	±5	
R44	Carbon	10K	¼	±5	
R45	Carbon	6.8K	¼	±5	
R46/47	Carbon	1K	¼	±5	
R48	Carbon	4.3K	¼	±5	

SWITCHES

Ref. No.	Description	R/S Part No.	Mfr's Part No.
S1	RESET SW		187010040A
S2	POWER SW		183110240A
S3	CHANNEL SW (AU only)		183110280A

INTEGRATED CIRCUITS

Ref. No.	Description		R/S Part No.	Manufacturer
U1	MC6803G or	(MCU)		MOTOROLA
	HD6803P			HITACHI
U2	SN74LS373N or	(D-LATCH)		MOTOROLA
	MB74LS373M			FUJITSU
U3	HN48364P or	(MASK ROM)		HITACHI
	MB8364M or			FUJITSU
	μPD2364C			NEC
U4	SN74LS155N or	(DECODER)		MOTOROLA
	MB74LS155M or			FUJITSU
	HD74LS155P			HITACHI
U5/6	SN74LS367AN or	(DRIVER)		MOTOROLA
	MB74LS367AM or			FUJITSU
	HD74LS367AP			HITACHI
U7	SN74LS245N or	(TRANSCEIVER)		MOTOROLA
	MB74LS245M or			FUJITSU
	HD74LS245P			HITACHI
U8	SN74LS174N or	(D-TYPE FF)		MOTOROLA
	MB74LS174M or			FUJITSU
	HD74LS174P			HITACHI
U9/10	MB8128-15P or	(STATIC RAM)		FUJITSU
	MSM2128-20RS or			OKI
	μPD4016C-1 or			NEC

Ref. No.	Description		R/S Part No.	Manufacturer
	μPD4016D-1			NEC
U11	MC6847P	(VDG)		MOTOROLA
U12	SN74LS14N or	(INVERTER)		MOTOROLA
	MB74LS14M			FUJITSU
U13	SN74LS32N or	(OR-GATE)		MOTOROLA
	MB74LS32M or			FUJITSU
	HD74LS32P			HITACHI
U14	MC14503BCP or	(BUFFER)		MOTOROLA
	HD14503BP or			HITACHI
	μPD4503BC or			NEC
	MSM4503RS			OKI
U15	LM339N or	(COMPARATOR)		MOTOROLA
	μPC339C			NEC
U16	MC1741CP1 or	(OP AMP)		MOTOROLA
	HA17741PS			HITACHI
U17	MC7805CT or	(VOLTAGE REGULATOR)		MOTOROLA
	NJM7805A or			JRC
	μPC7805H			NEC
U18	SN74LS74AN or	(D-FF)		MOTOROLA
	MB74LS74AM or			FUJITSU
	HD74LS74AP			HITACHI
U19	SN74LS76AN or	(JK-FF)		MOTOROLA
	MB74LS76AM or			FUJITSU
	HD74LS76P			HITACHI
U20	SN74LS02N or	(NOR-GATE)		MOTOROLA
	MB74LS02M or			FUJITSU
	HD74LS02P			HITACHI
U21	TCC1000	(PAL LOGIC)		HITACHI
U22	MC1372P (SC77538)	(VIDEO MODULATOR)		MOTOROLA
U23	LM319N	(DUAL COMPARATOR)		NS
U24	NJM4560D	(OP AMP)		JRC
U25	NJM79L05A or	(VOLTAGE REGULATOR)		JRC
	MC79L05ACP			MOTOROLA

CRYSTALS

Ref. No.	Description	R/S Part No.	Mfr's Part No.
X1	HC-18/U 4.433618MHz		391010251A
X2	HC-18/U 3.5593835MHz		391010460A

EXPLODED VIEW PARTS LIST

Ref. No.	Description	R/S Part No.	Mfr's Part No.
1	Cabinet Ass'y, Top		M00324
	Cabinet, Top		601210420A
	Plate, Model		711010040B
2	Cover, Connector		851210720A
3	Key Board Ass'y		187510010A
4	Knob, Reset (Red)		659510310A
5	Holder, SW Reset		411101870A
6	Not used		
7	P.C. Board Ass'y		U32011
7	P.C. Board Ass'y (AU only)		U32011
8	Modulator, (Custom) (BG/UK)		525010040A
	Modulator, (Custom) (AU only)		525010050A
9	Connector, Flat Wire		193904400A
10	Sheet, Shield		473310510B
11	Knob, Channel (Black) (AU only)		659510320A
12	Cabinet, Bottom		601310290C
13	Foot, Rubber		608010080A
F1	Screw, Tap Tite 3x12 BT-B For Cabinet		
F2	Screw, Tap Tite 3x 8 BT-B For Key Board		
F3	Screw, Tap Tite 3x 8 PT-B For P.C. Board		
F4	Screw, Tap Tite 3x 6 PT-B For Cover		
F5	Rivet For Sheet, Shield		HARRA003SN

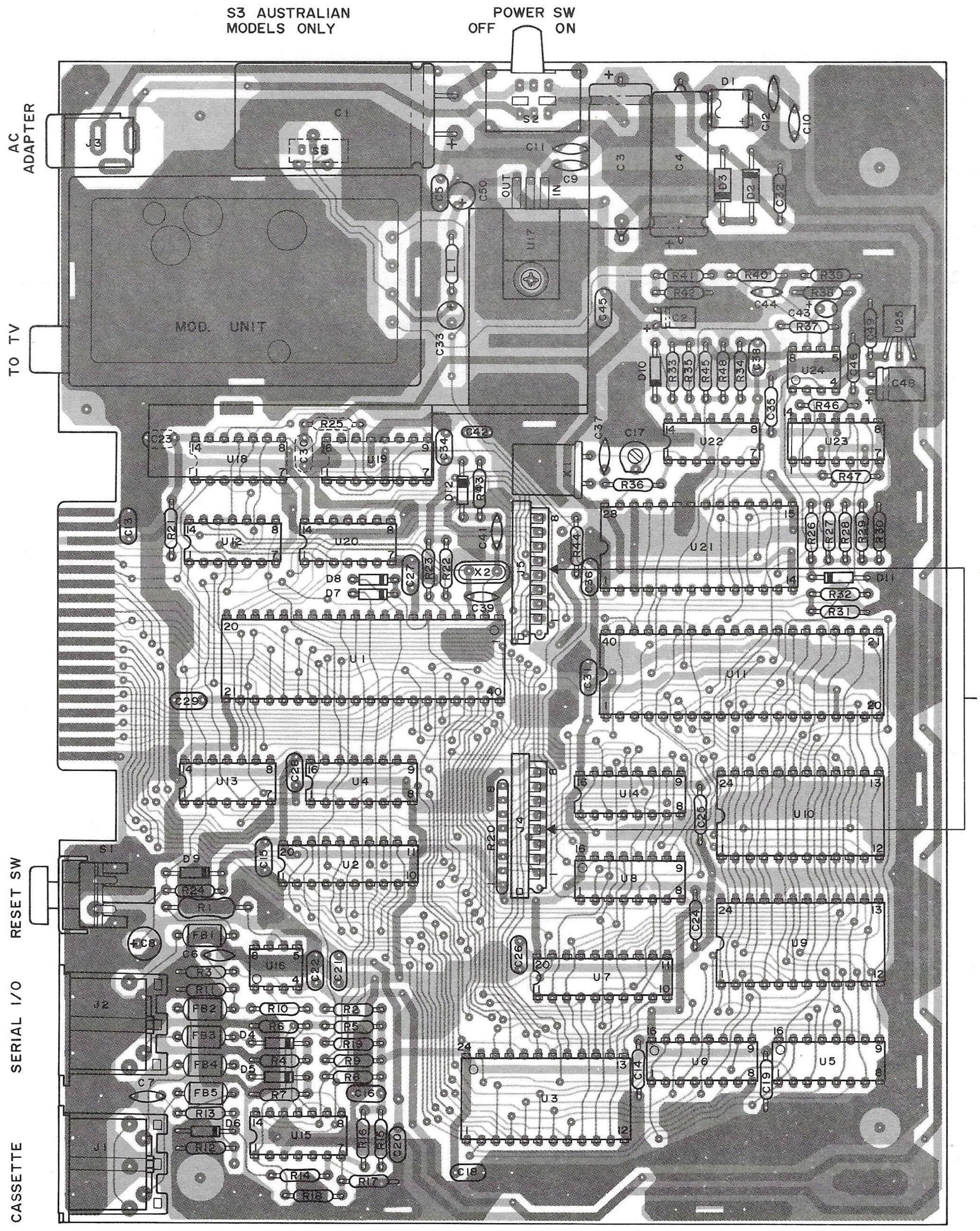
MISCELLANEOUS PARTS LIST

Ref. No.	Description	R/S Part No.	Mfr's Part No.
	Adaptor, Power AC-DC (BG)		10901012DA
	AC-DC (UK)		10901011DA
	AC-DC (AU)		10901013DA
	Cord, Patch		313510080A

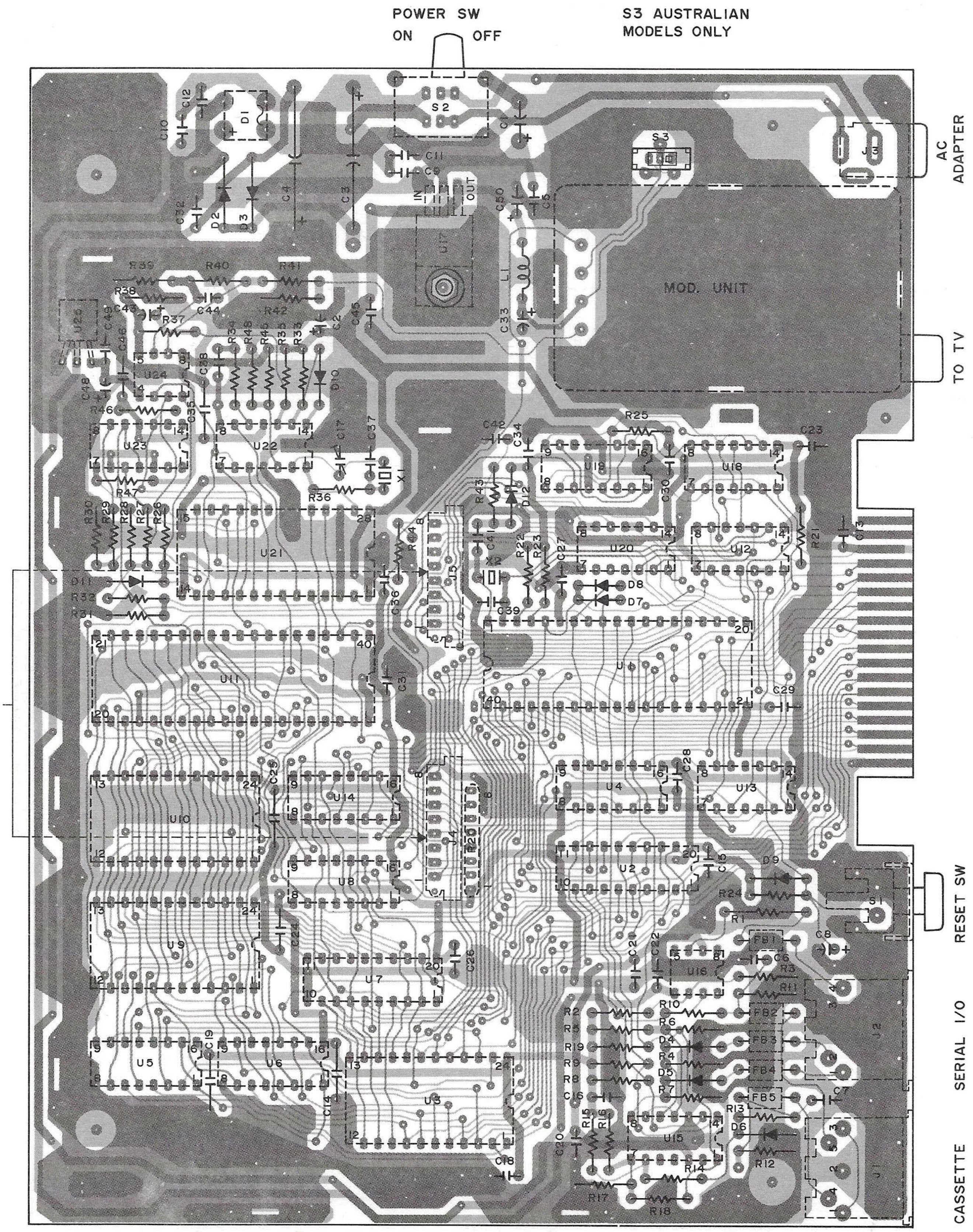
SECTION VII

PRINTED CIRCUIT BOARDS

MAIN P.C.B.
(TOP VIEW)



(BOTTOM VIEW)



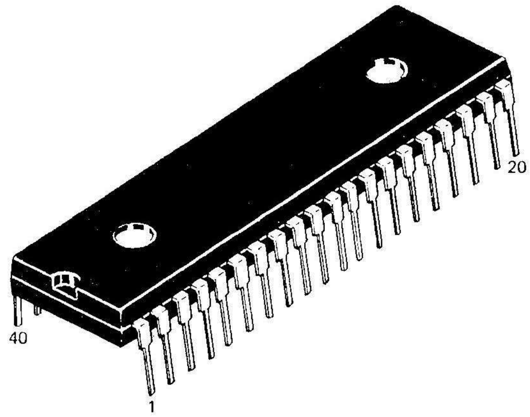
POWER SW
ON
OFF
S3 AUSTRALIAN
MODELS ONLY
AC
ADAPTER
MOD. UNIT
TO TV
FROM KEY BOARD
RESET SW
SERIAL I/O
CASSETTE

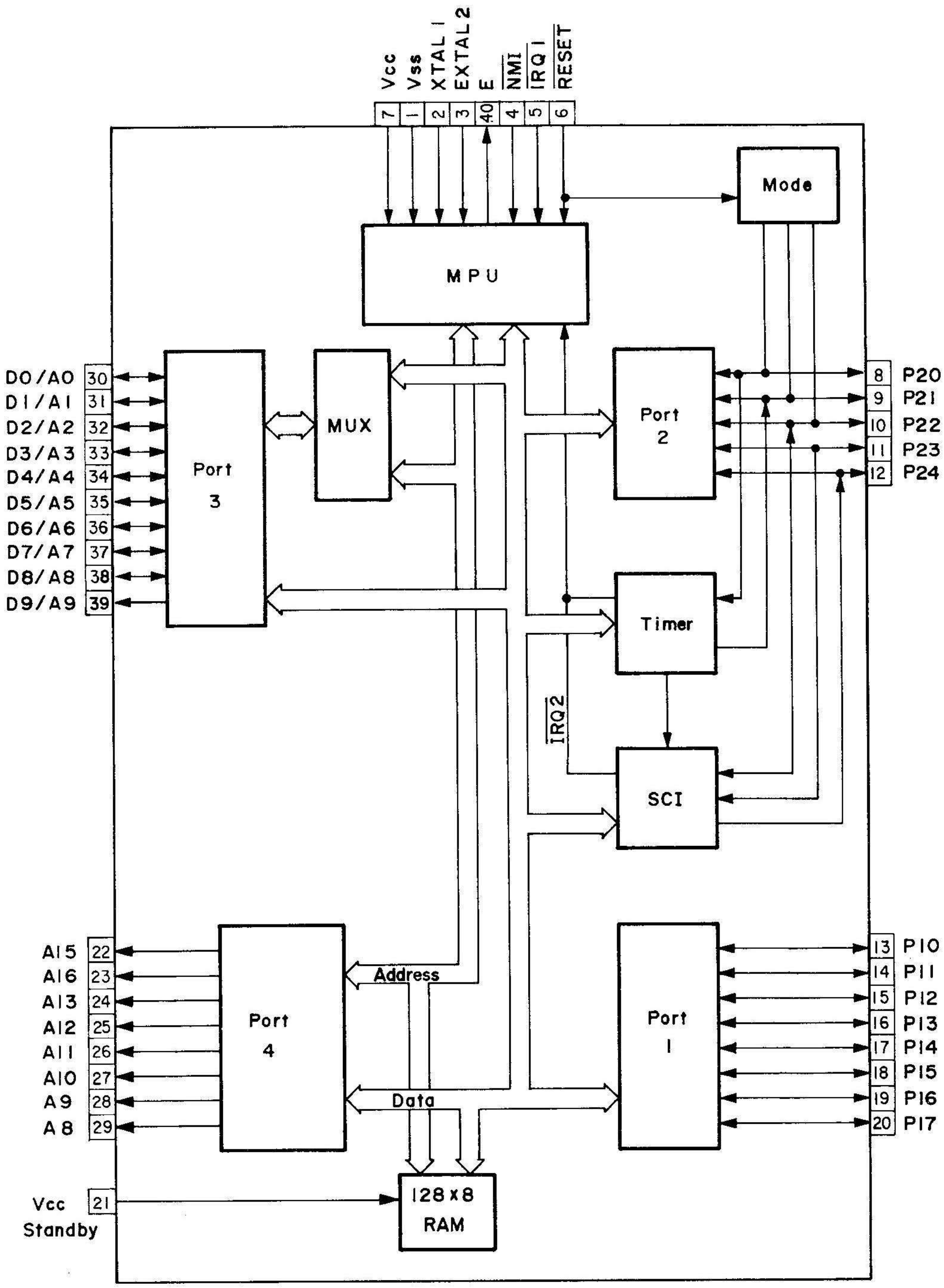
SECTION VIII

IC INTERNAL CONNECTIONS

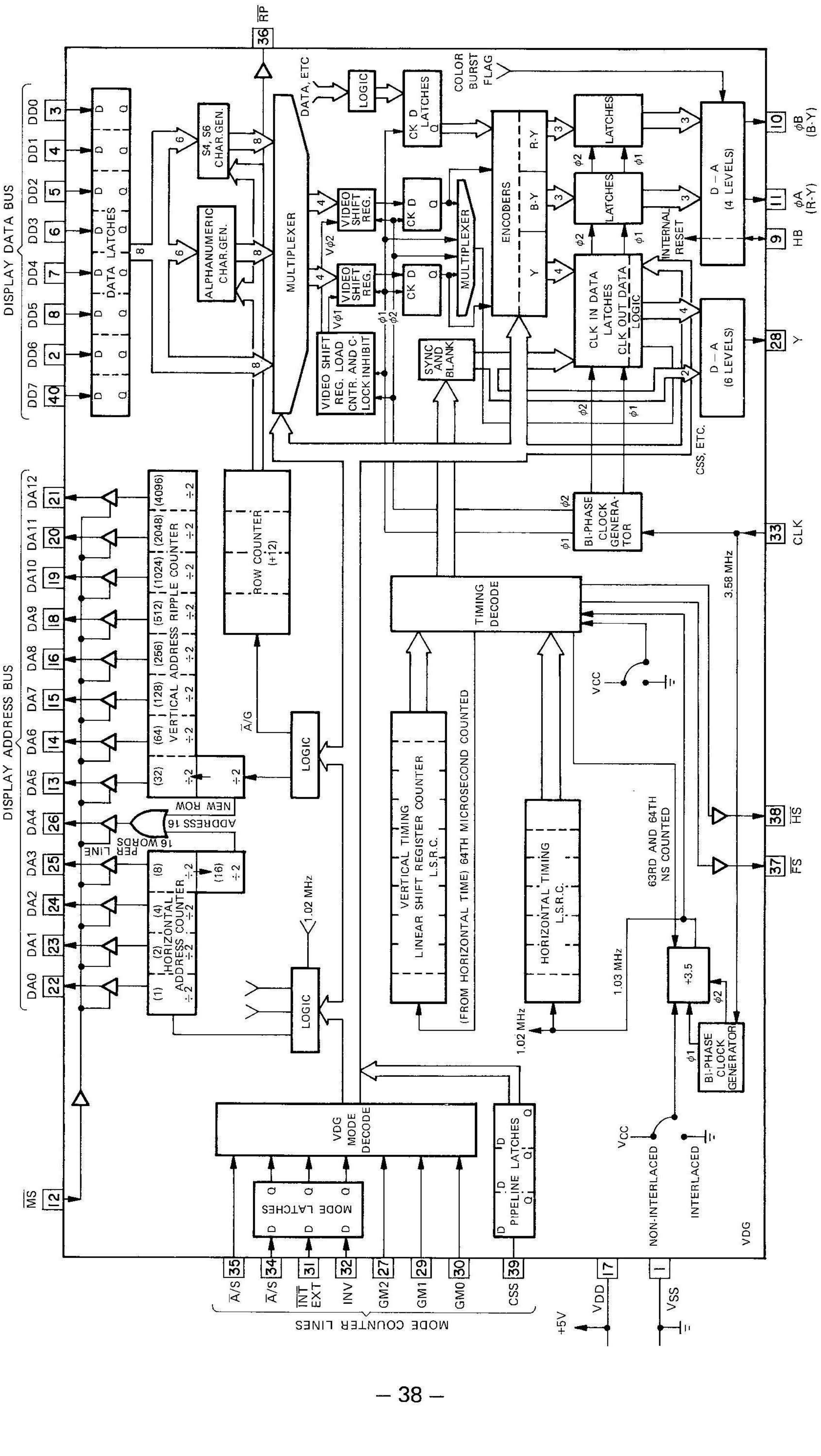
IC INTERNAL CONNECTIONS

U1 MC6803G (Motorola) or HD6803P (Hitachi)

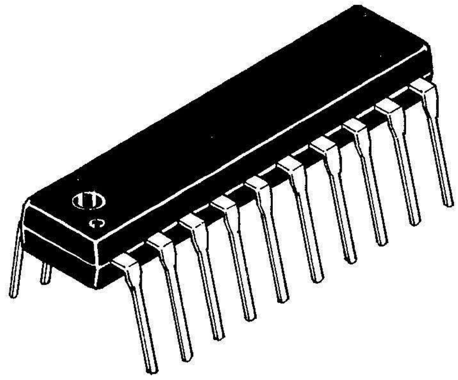


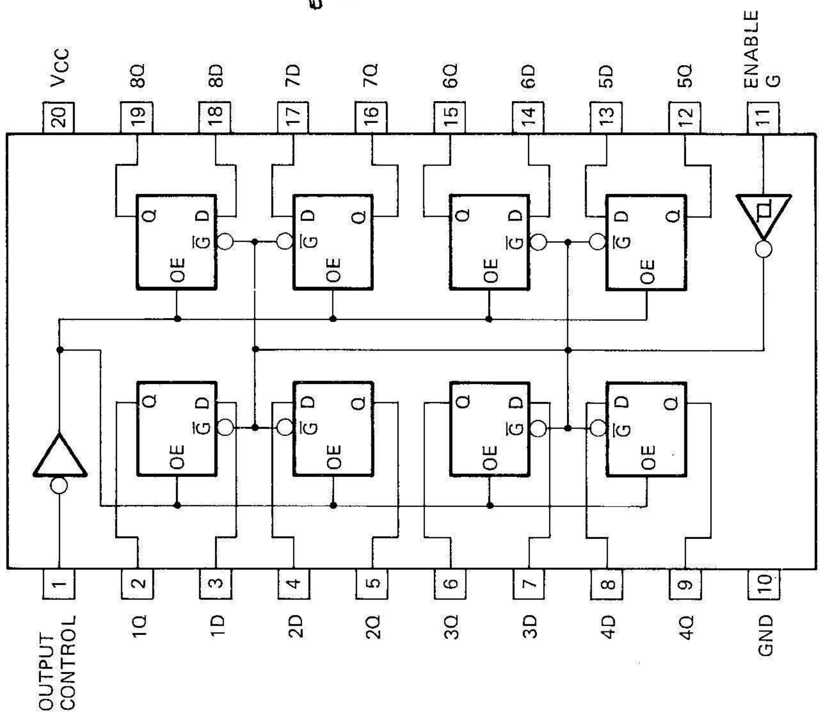


U11 MC6847P (Motorola)

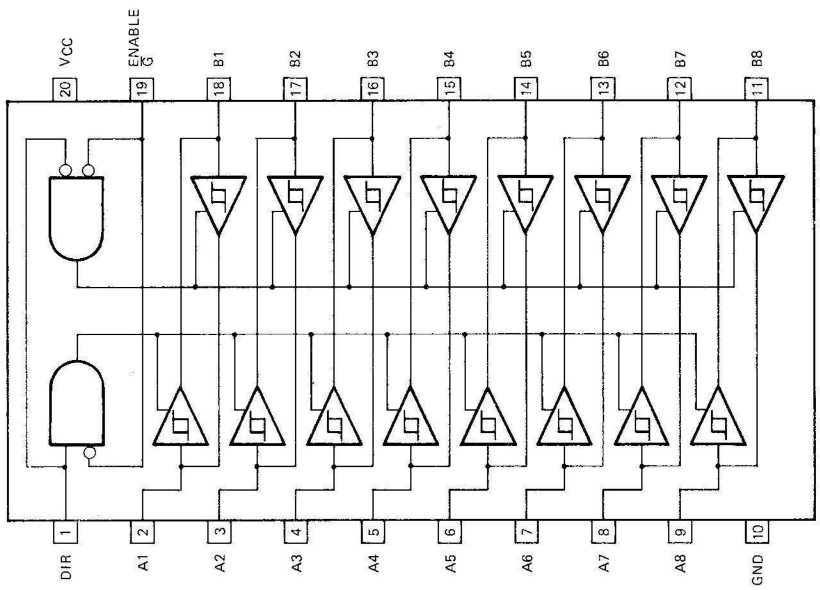


U2 SN74LS373N (Motorola) or MB74LS373M (Fujitsu)

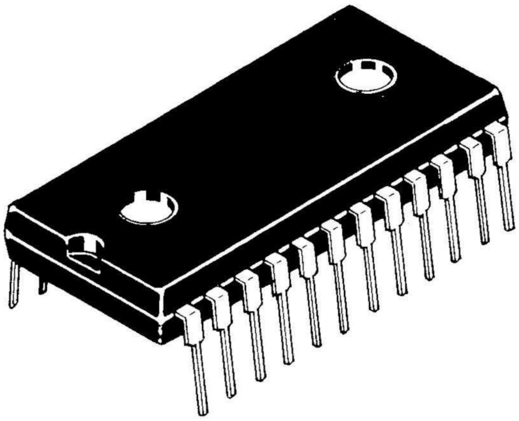


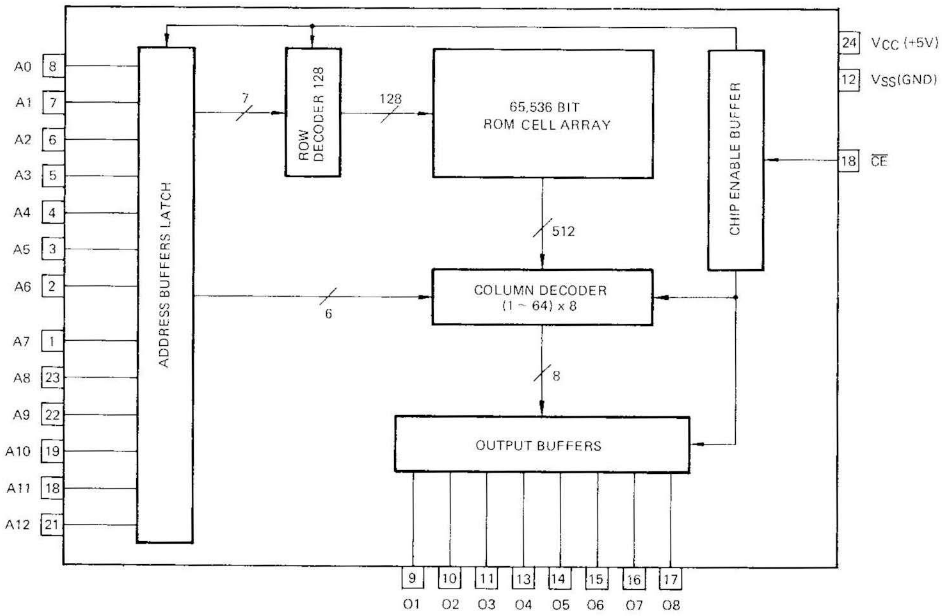


U7 SN74LS245N (Motorola) or MB74LS245M (Fujitsu) or HD74LS245P (Hitachi)

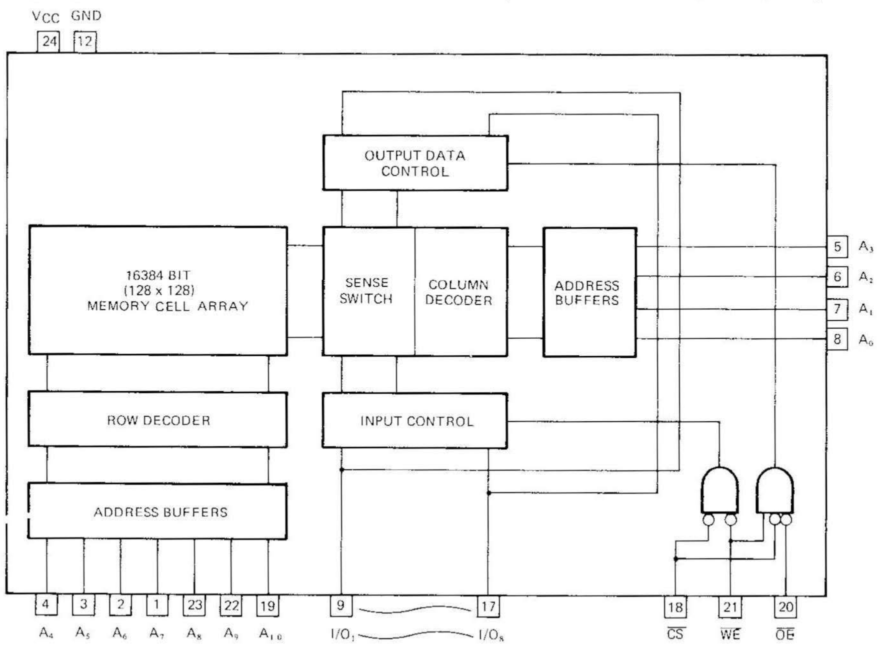


U3 HN48364P (Hitachi) or MB8364M (Fujitsu) or μPD2364C (NEC)

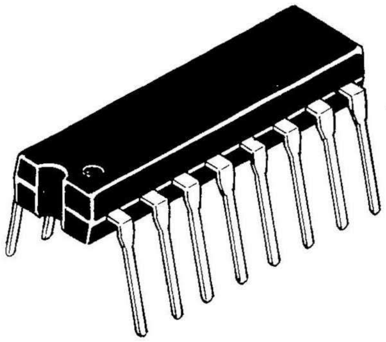


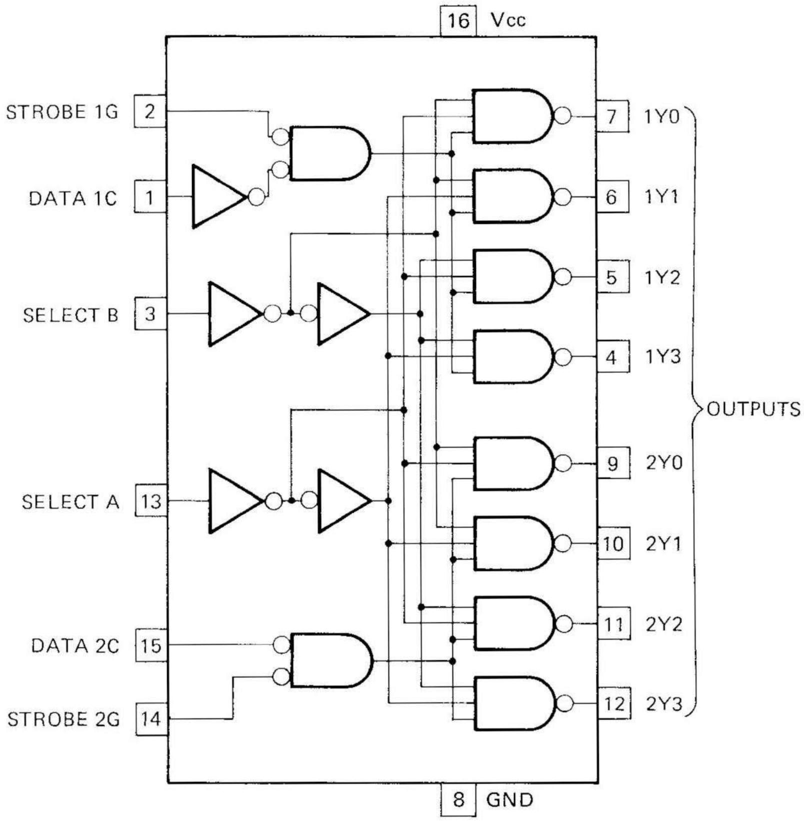


U9/10 MB8128-15P (Fujitsu) or MSM2128-20RS (Oki) or μPD40160C-1 (NEC) or μPD4016D-1 (NEC)

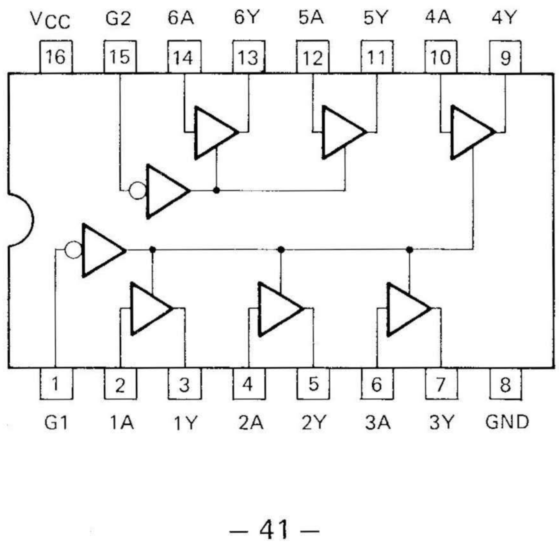


U4 SN74LS155N (Motorola) or MB74LS155M (Fujitsu) or HD74LS155P (Hitachi)





U5/U6 SN74LS367AN (Motorola) or MB74LS367AM (Fujitsu) or HD74LS367AP (Hitachi)



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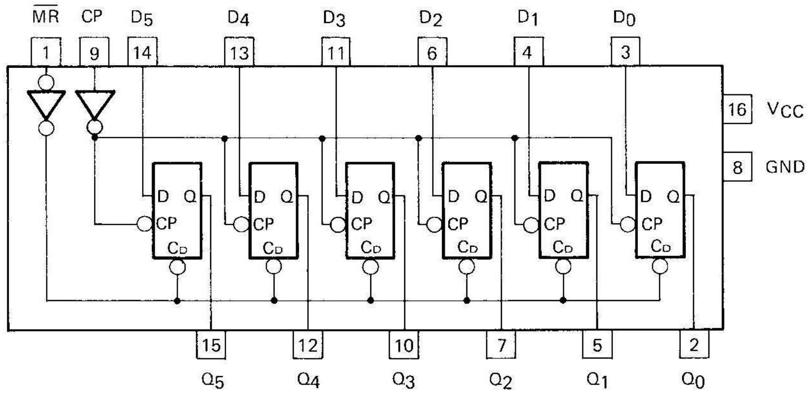
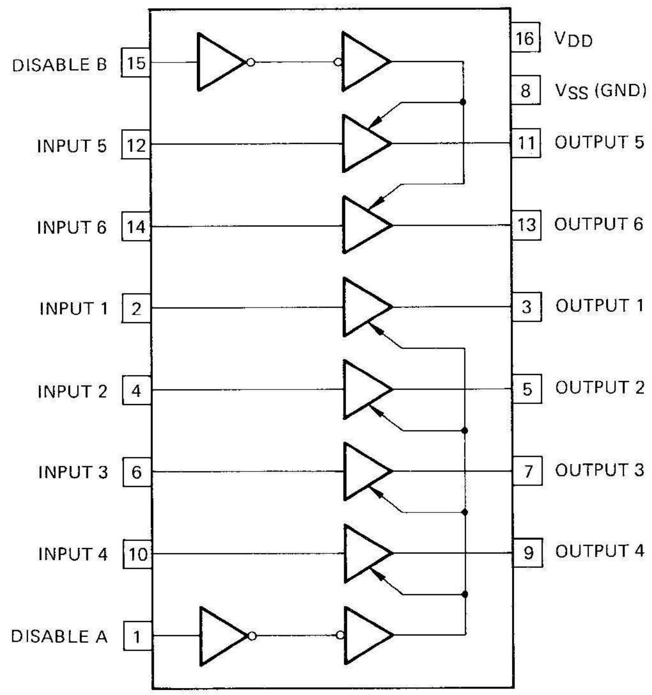
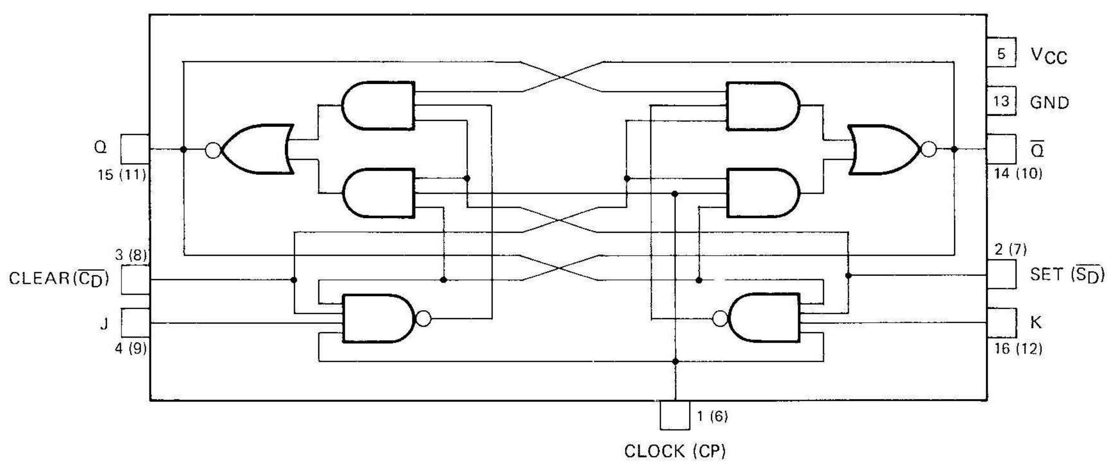


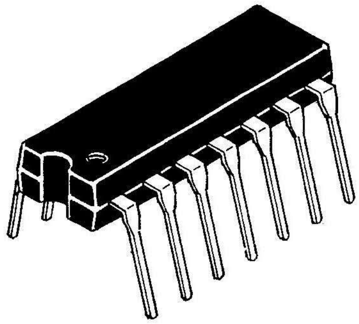
U14 MC14503BCP (Motorola) or HD14503BP (Hitachi) or μPD4503BC (NEC) or MSM4503RS(Oki

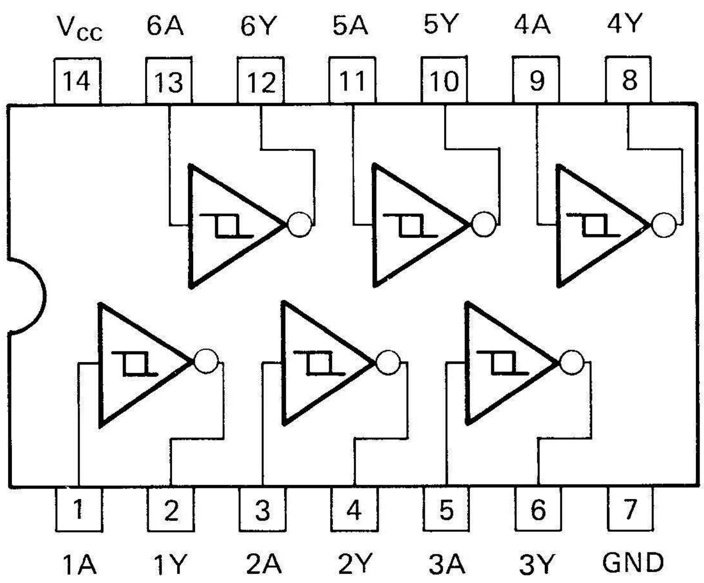


U19 SN74LS76AN (Motorola) or MB74LS76AM (Fujitsu) or HD74LS76P (Hitachi)



U12 SN74LS14N (Motorola) or MB74LS14M (Fujitsu)





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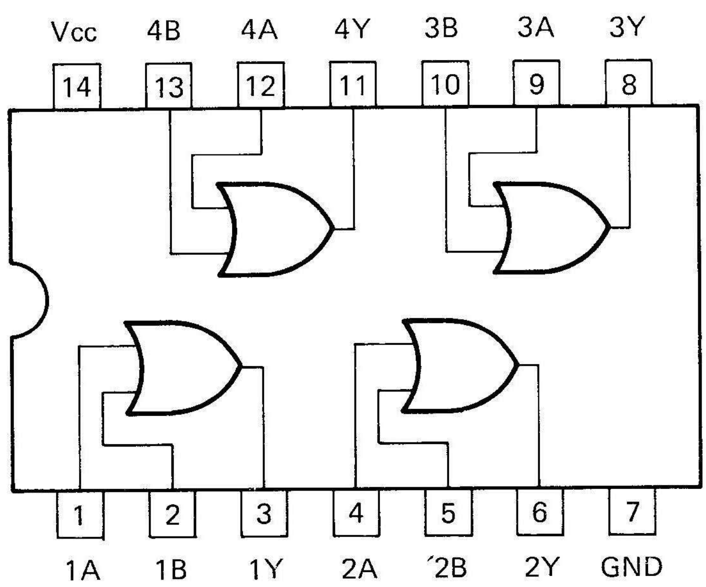
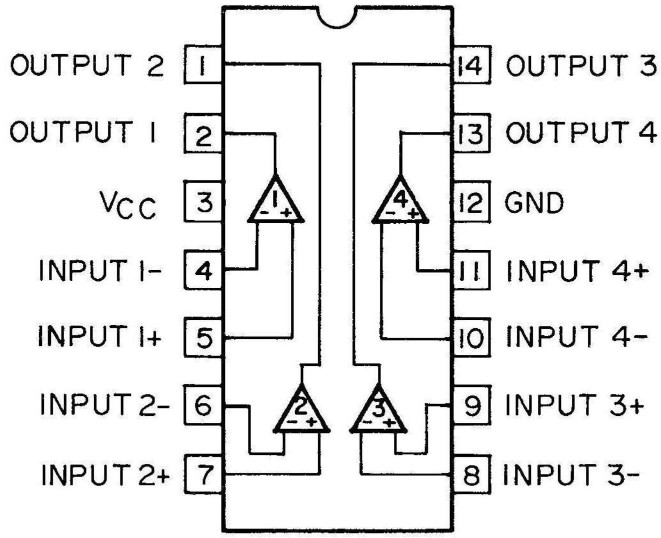
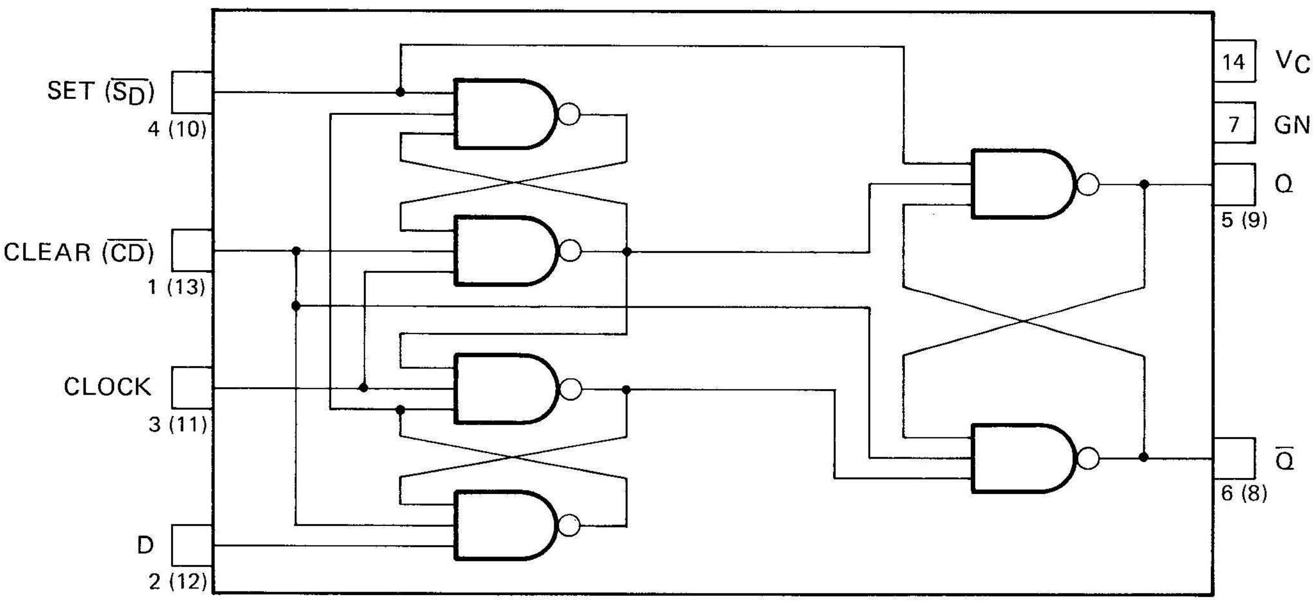


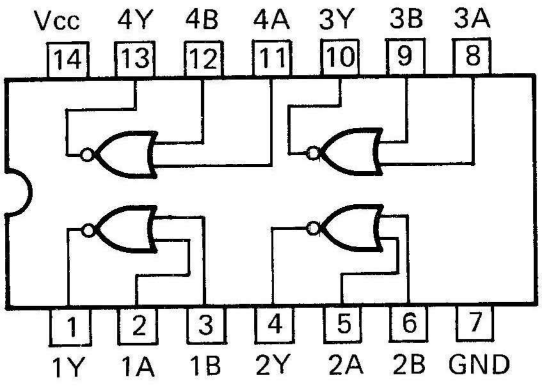
U15 LM339N (Motorola) or μPC339C (NEC)



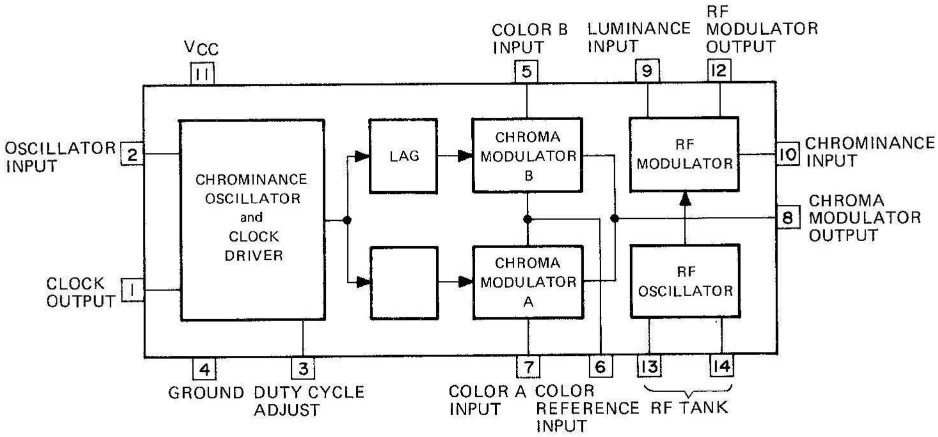
U18 SN74LS74AN (Motorola) or MB74LS74AM (Fujitsu) or HD74LS74AP (Hitachi)



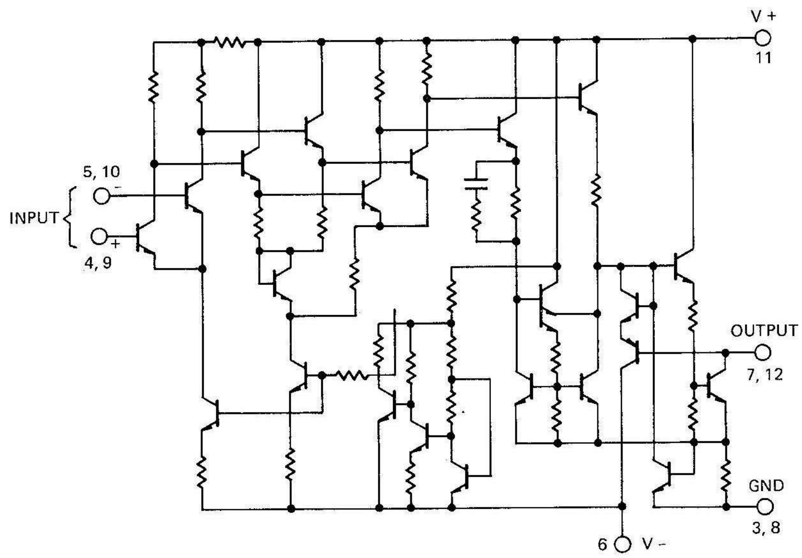
U20 SN74LS02N (Motorola) or MB74LS02N (Fujitsu) or HD74LS02P (Hitachi)



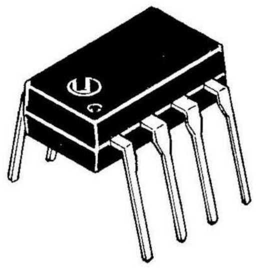
U22 MC1372P(SC77538) (Motorola)

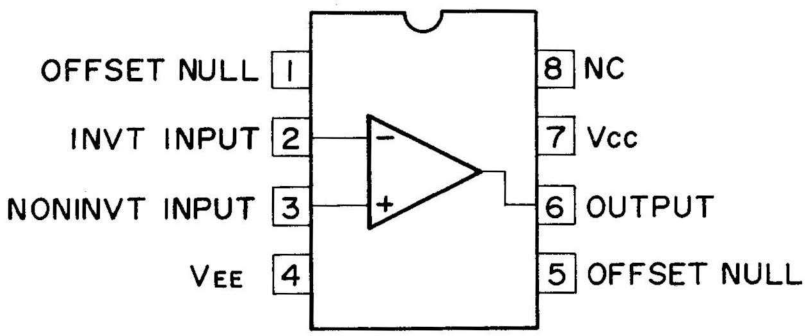


U23 LM319N (NS)

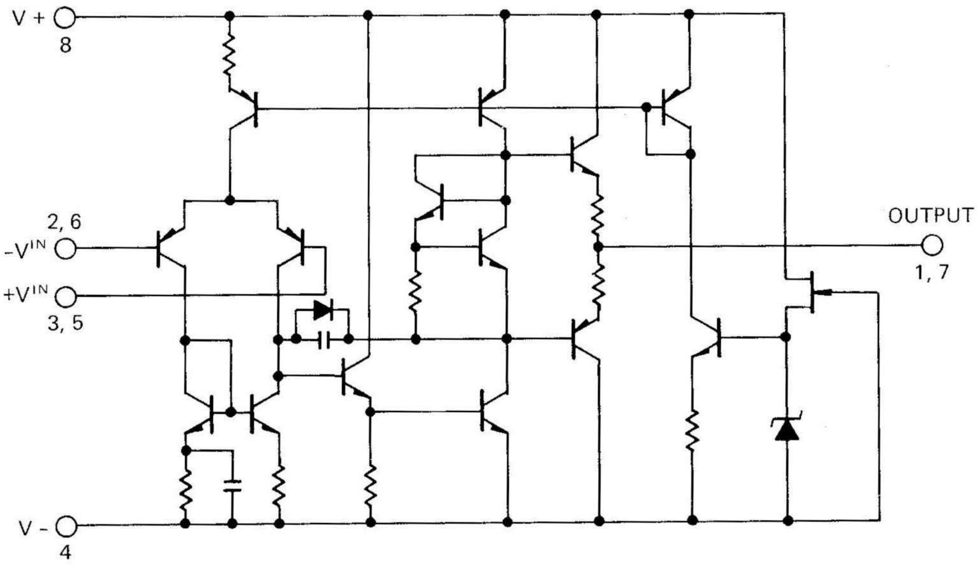


U16 MC1741CP1 (Motorola) or HA17741PS (Hitachi)

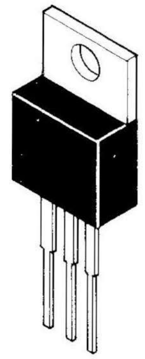


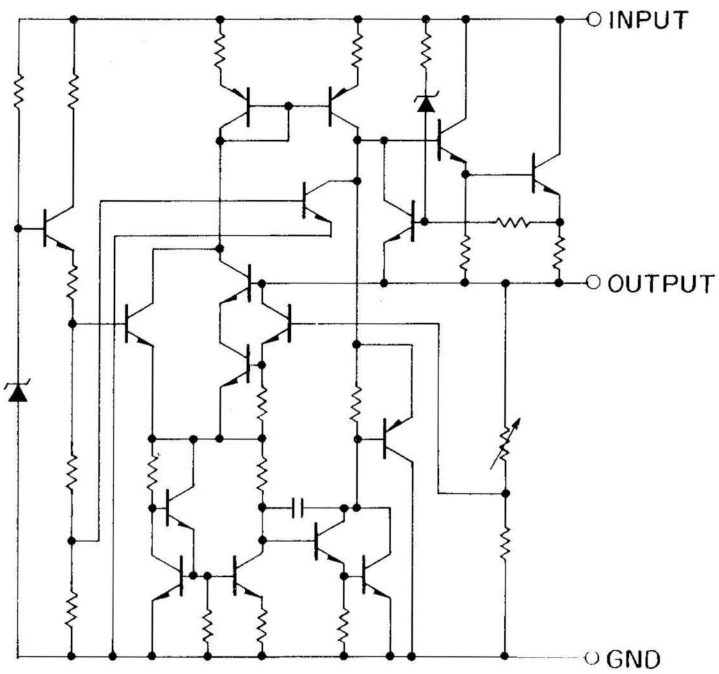


U24 NJM4560D (JRC)

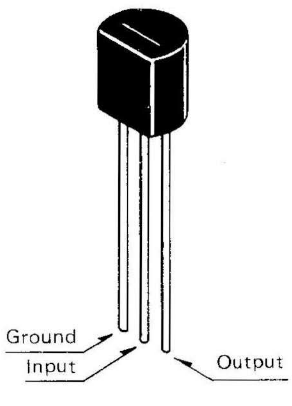


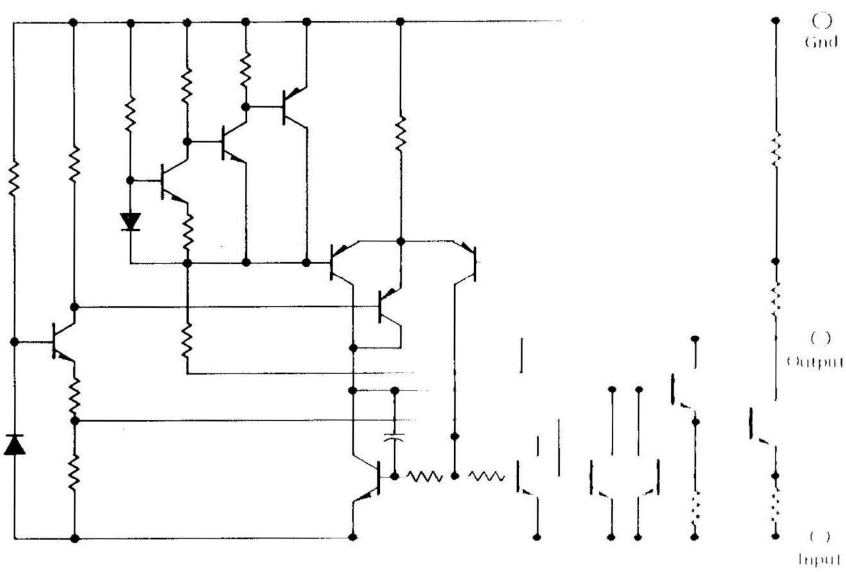
U17 MC7805CT (Motorola) or NJM7805A (JRC) or μPC7805H (NEC)



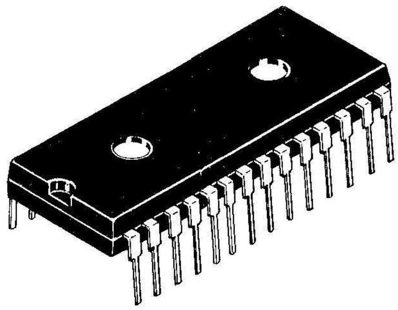


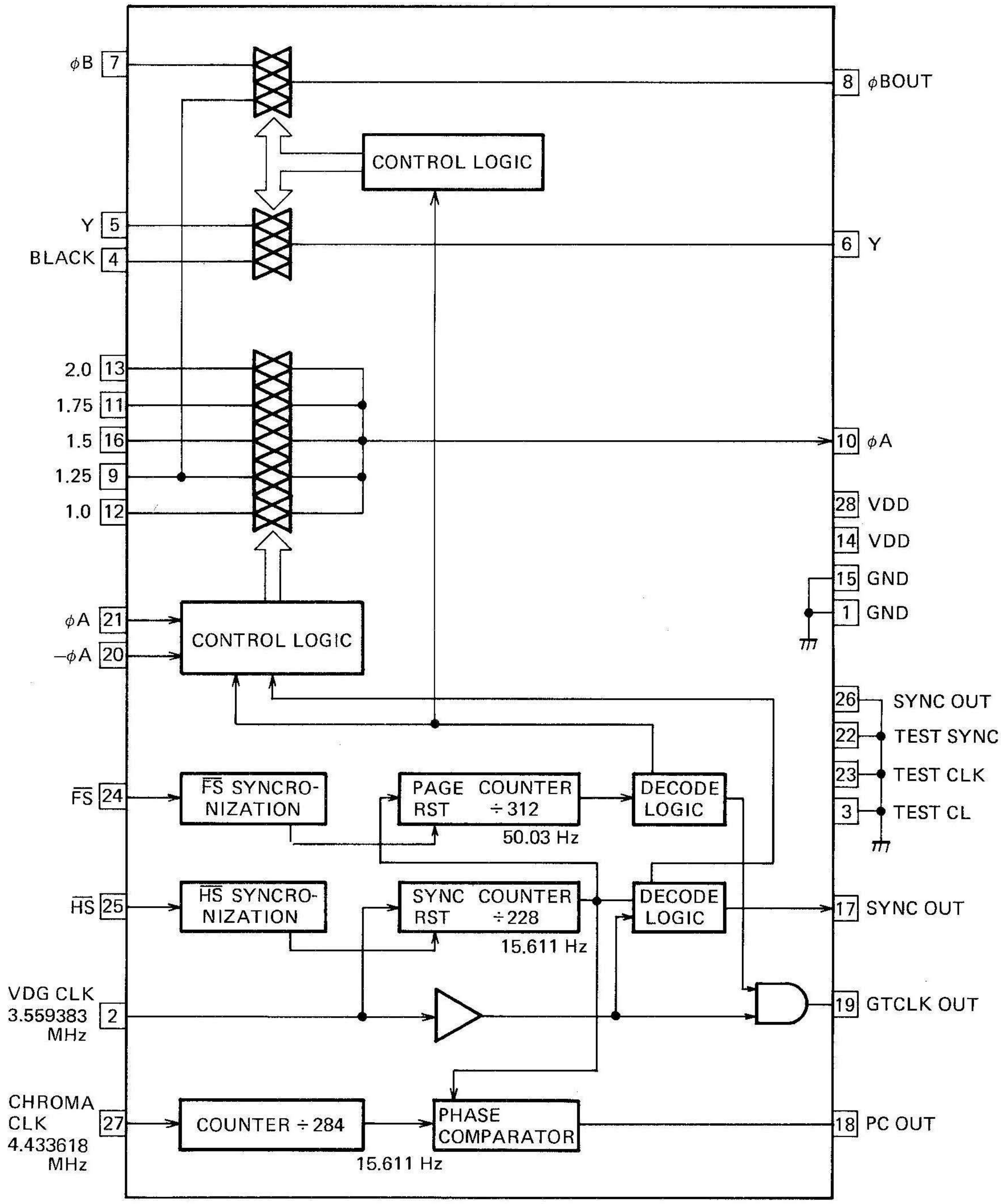
U25 NJM79L05 (JRC) or MC79L05ACP (Motorola)





U21 TCC1000 (Hitachi)





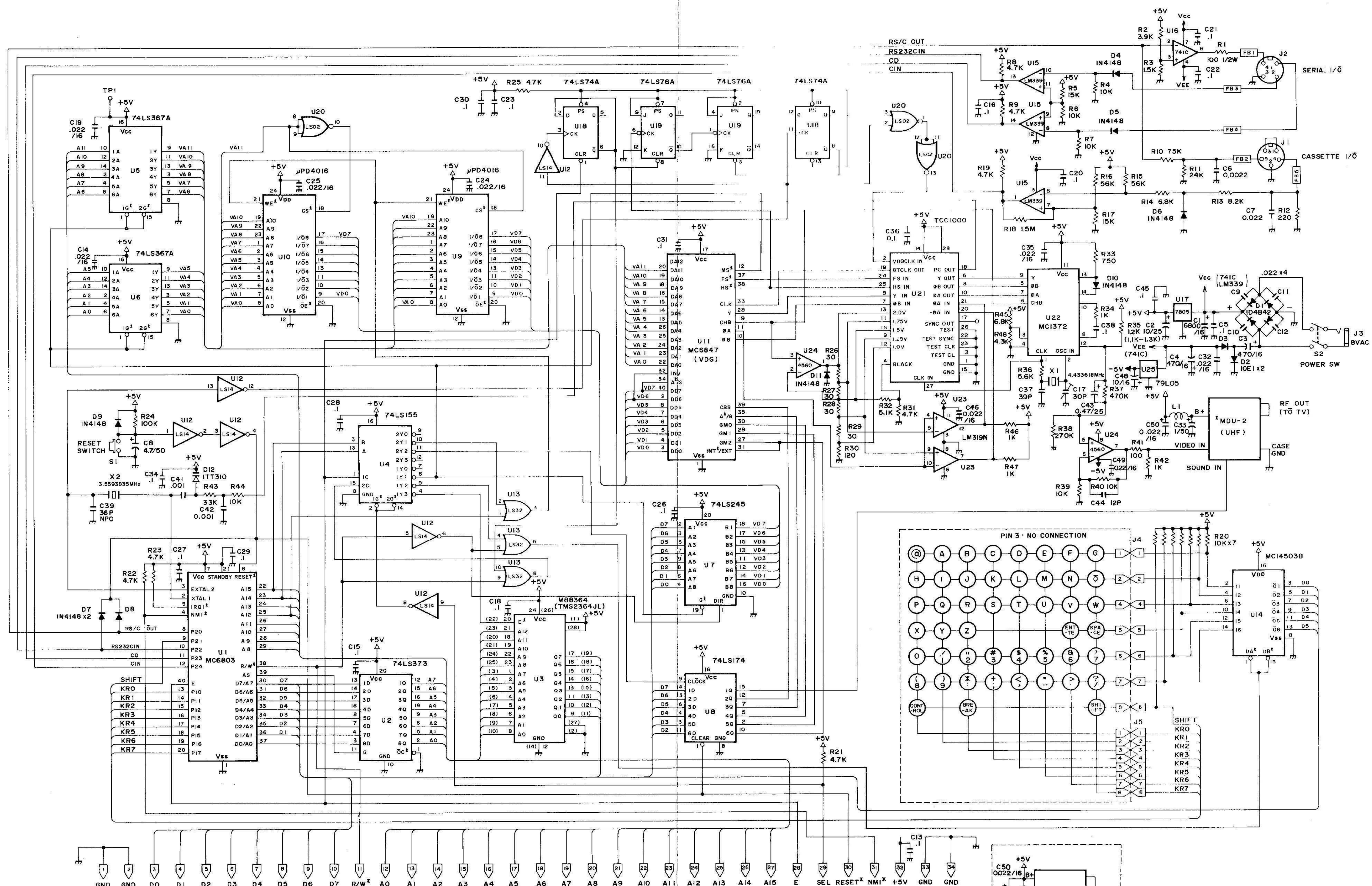
SECTION IX

SCHEMATIC DIAGRAM

SECTION X

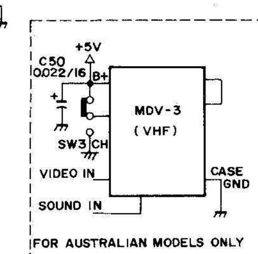
EXPLODED VIEW

SCHEMATIC DIAGRAM

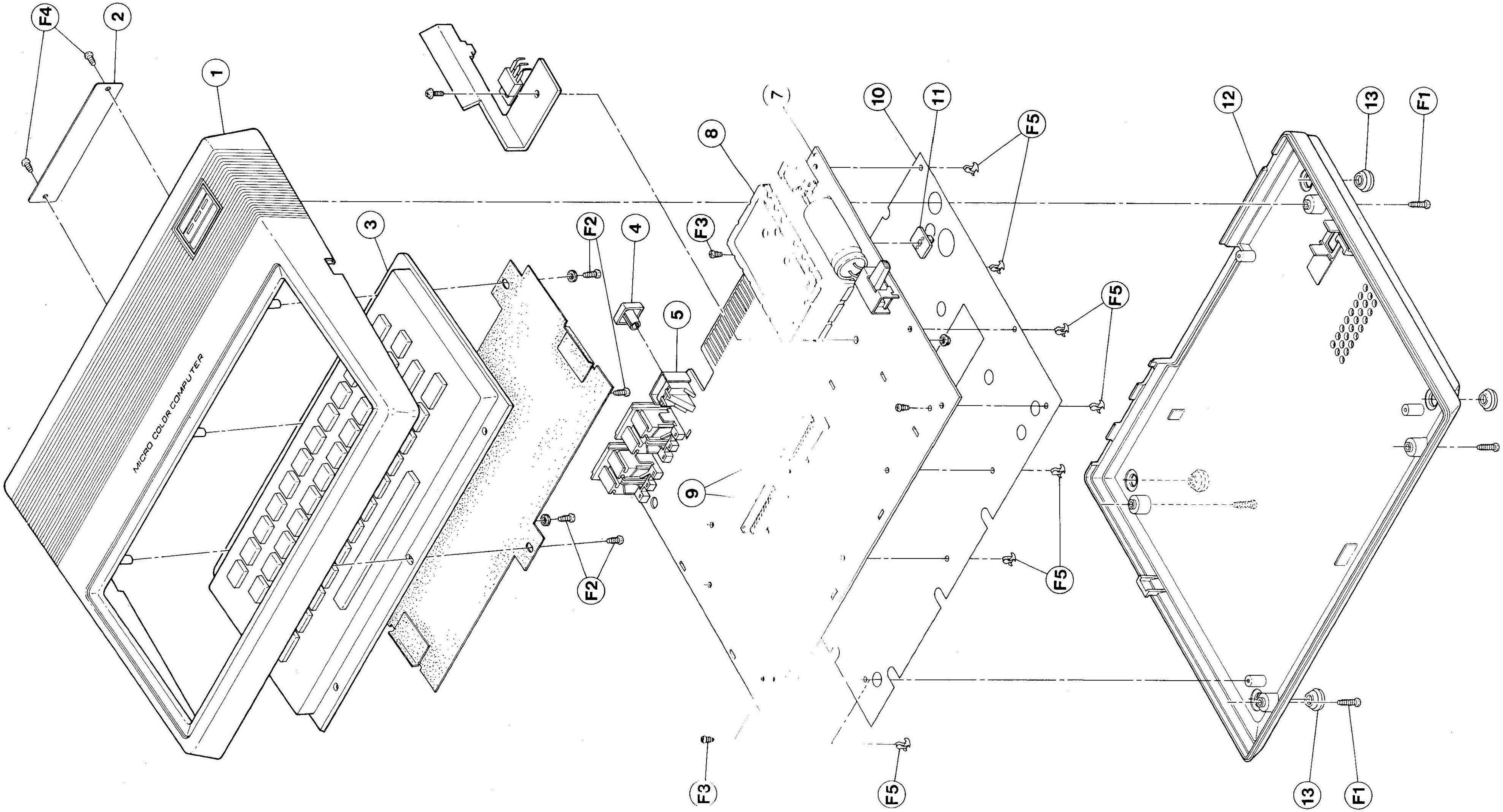


NOTES:- (1) ALL RESISTANCE VALUES ARE INDICATED IN "OHM" ($K=10^3$ OHM, $M=10^6$ OHM)

(2) ALL CAPACITANCE VALUES ARE INDICATED IN "µF" ($P=10^{-6}$µF)



EXPLODED VIEW



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